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# MS-7850 ATX Ver: 11

Intel -ShakeBay plamform

CPU:

INTEL-Haswell LGA1150

CPU DISPLAY

HDMI(portB) DVI (port C)

System Chipset:

INTEL-LYNX

OnBoard Chipset:

HD Audio Codec:ALC887 Co-lay 892

LAN-RTL8111G Co-lay 8106G

SIO:Nuvoton NCT6779

Main Memory:

DDRIII (1066/1333/1600MHz) \* 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 2

PCI Slot \* 2

PWM:

VRD12 - ISL95812( 3 Phase 12MOS , Power pak)

Other:

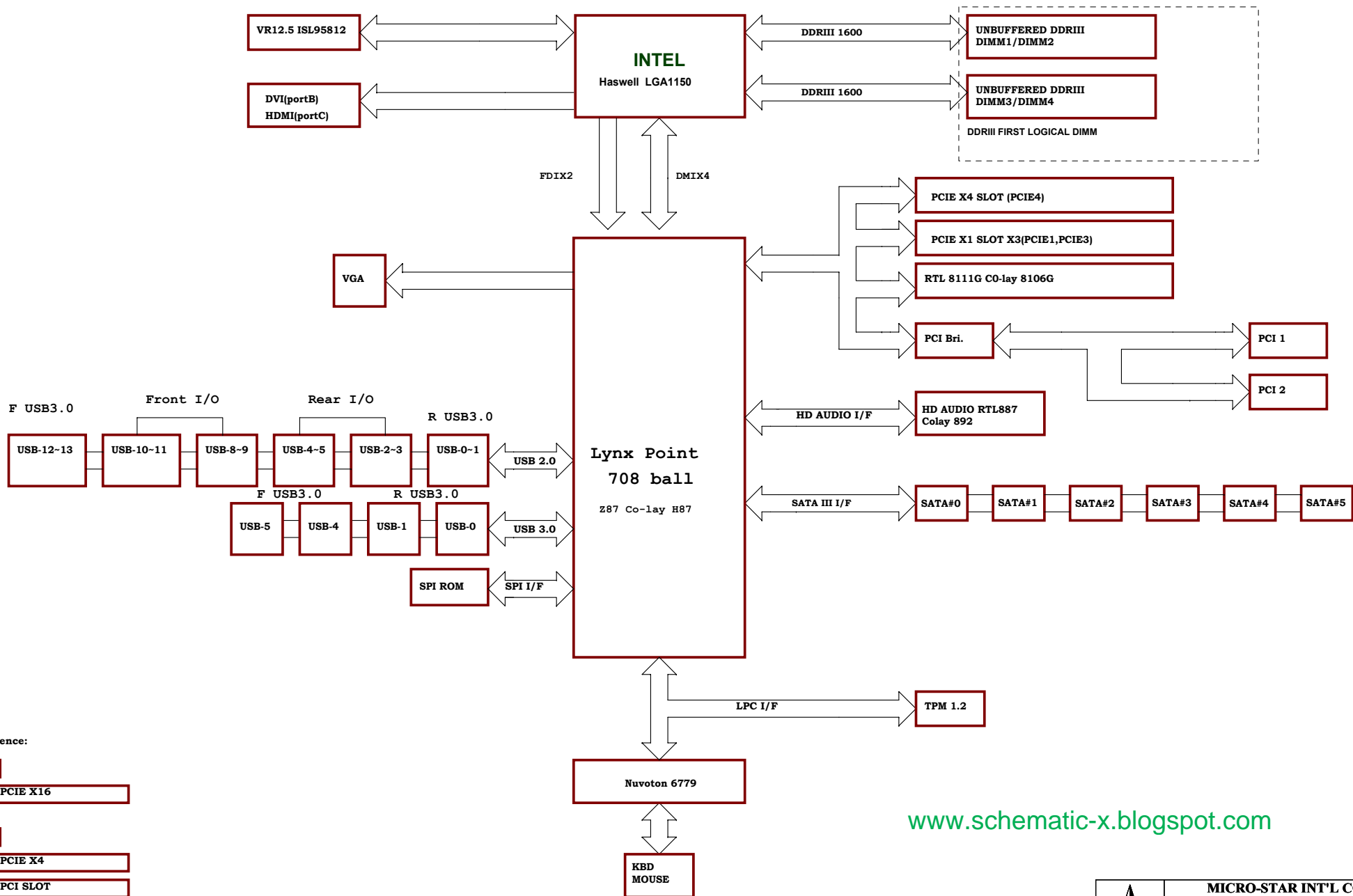
SATA(SATA3-500MB/s) \*6

REAL USB2.0 \*4

FRONT USB2.0 \*4

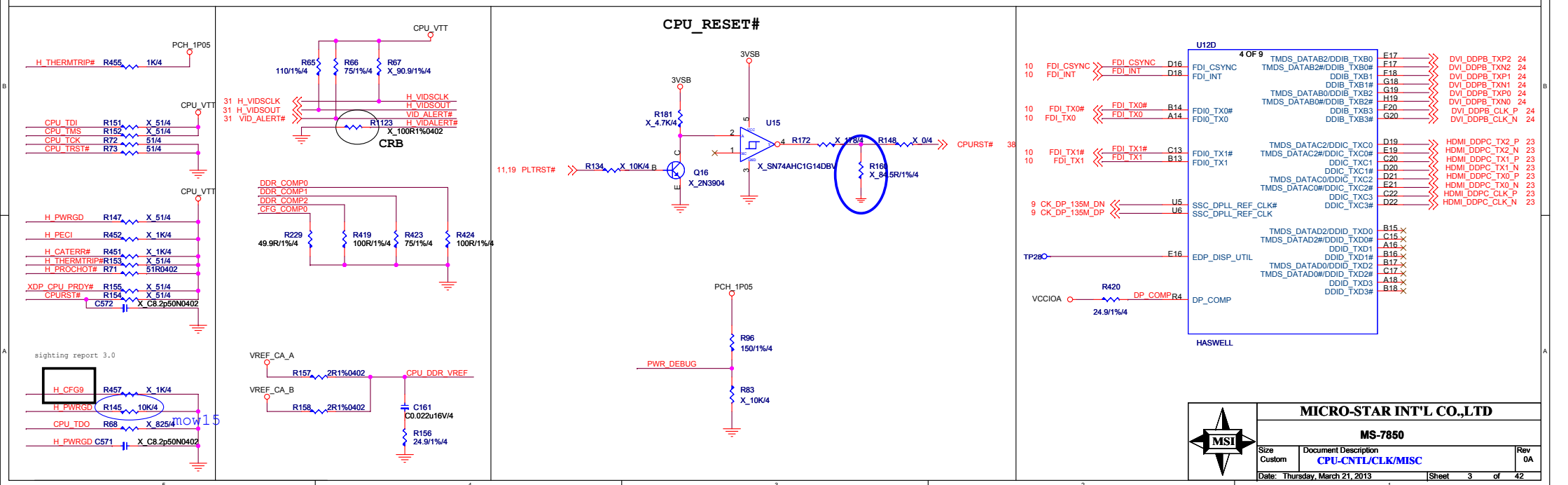
REAL USB3.0 \*2

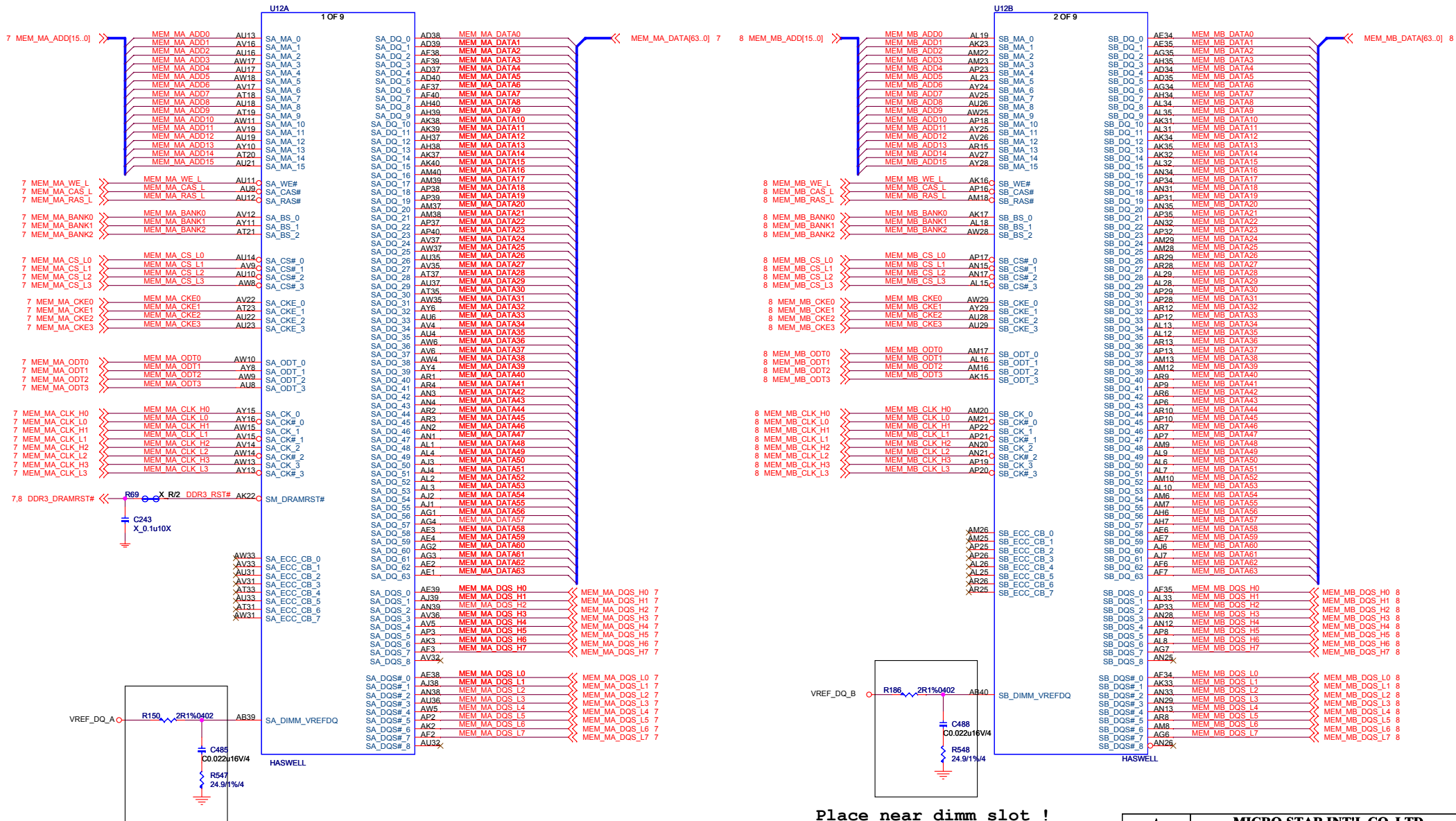
FRONT USB3.0 \*2



- Slot Sequence:
- PCIE X1
  - PCIE X16
  - PCIE X1
  - PCIE X4
  - PCI SLOT
  - PCI SLOT

[www.schematic-x.blogspot.com](http://www.schematic-x.blogspot.com)





Place near dimm slot !

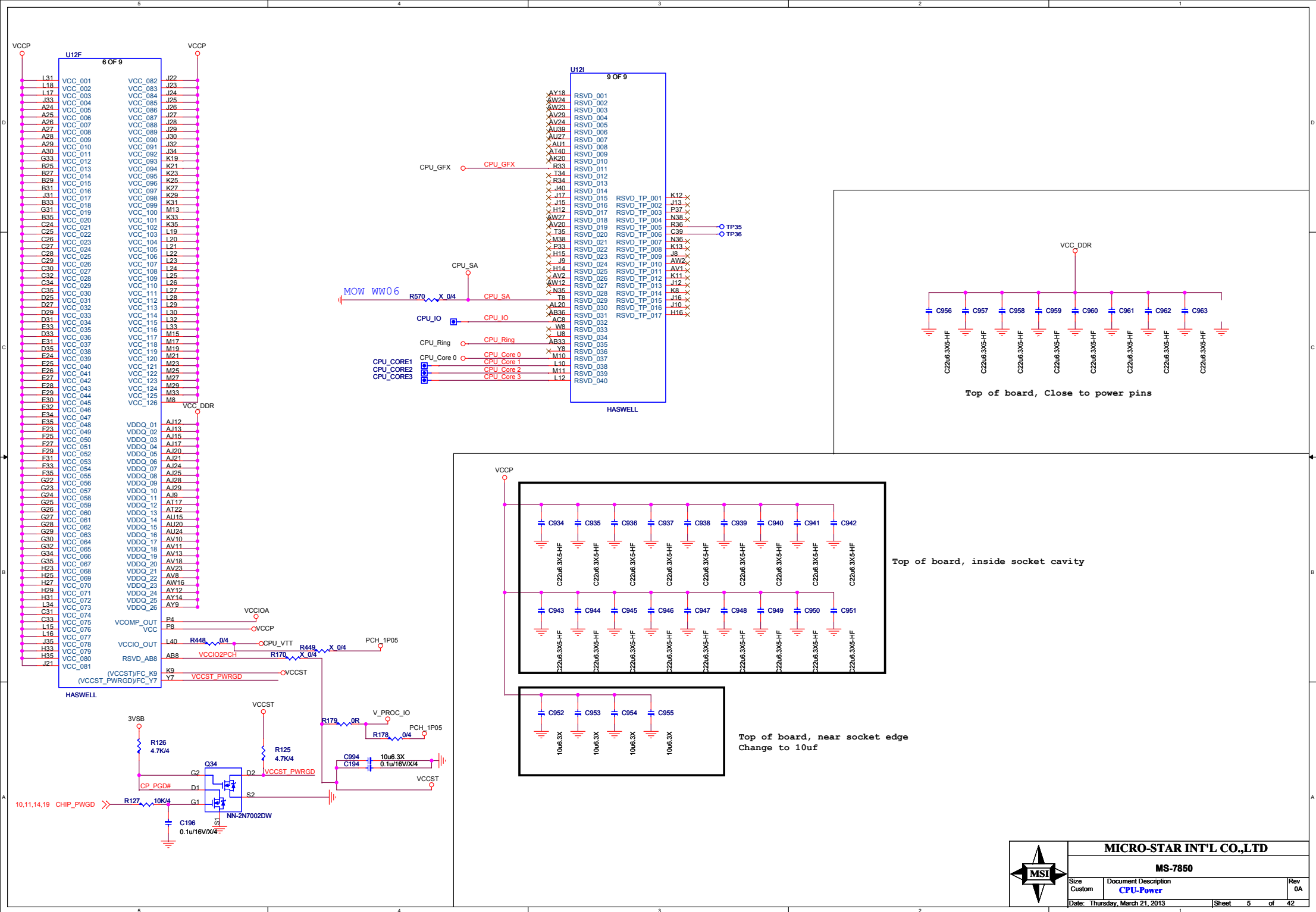
Place near dimm slot !



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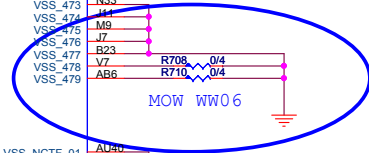
MS-7850

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GND

GND



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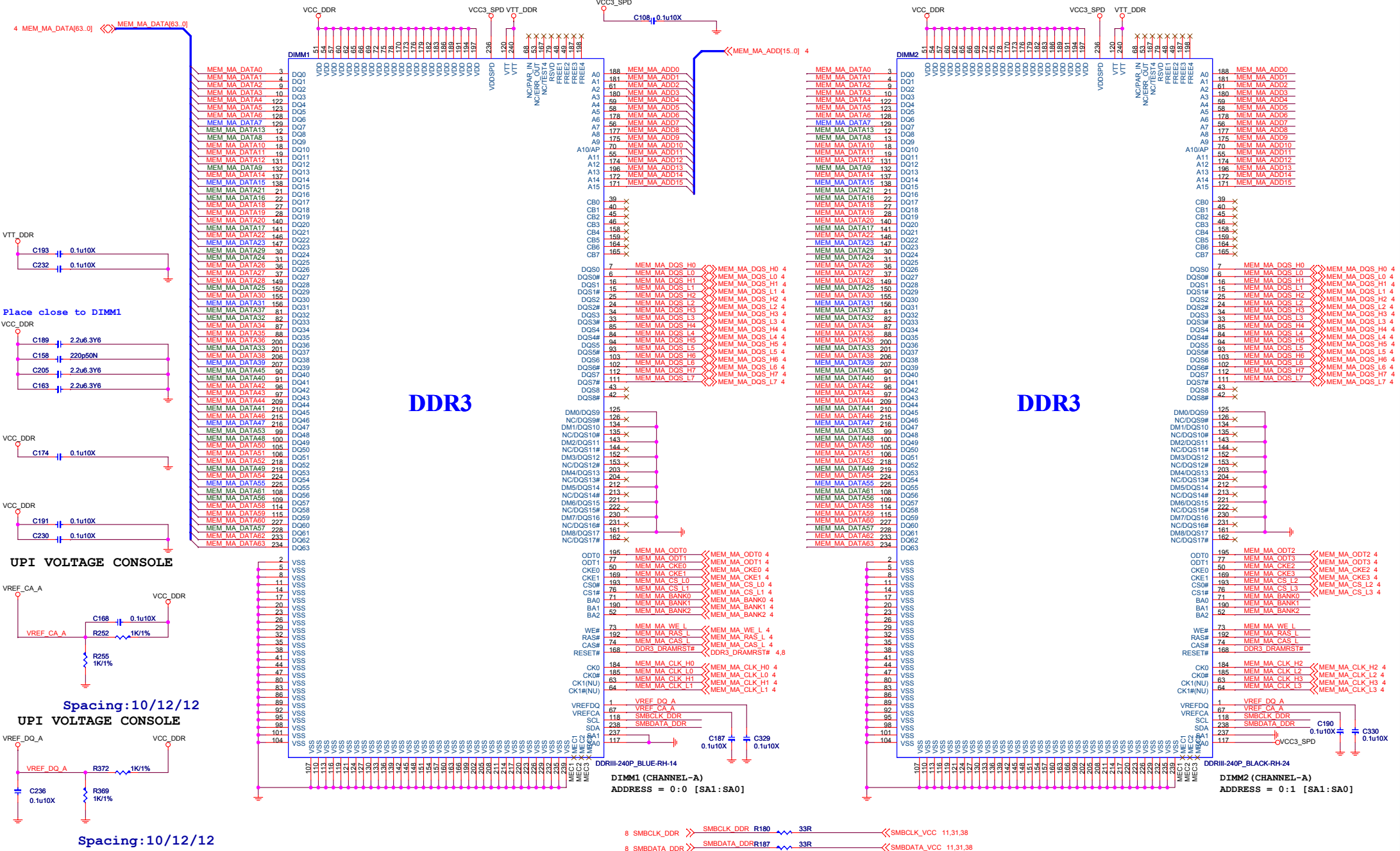
MS-7850

Size	Document Description	Rev
Custom	CPU-GND	0A
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# DDRIII DIMM\_A0

# DDRIII DIMM\_A1



DDR3

DDR3



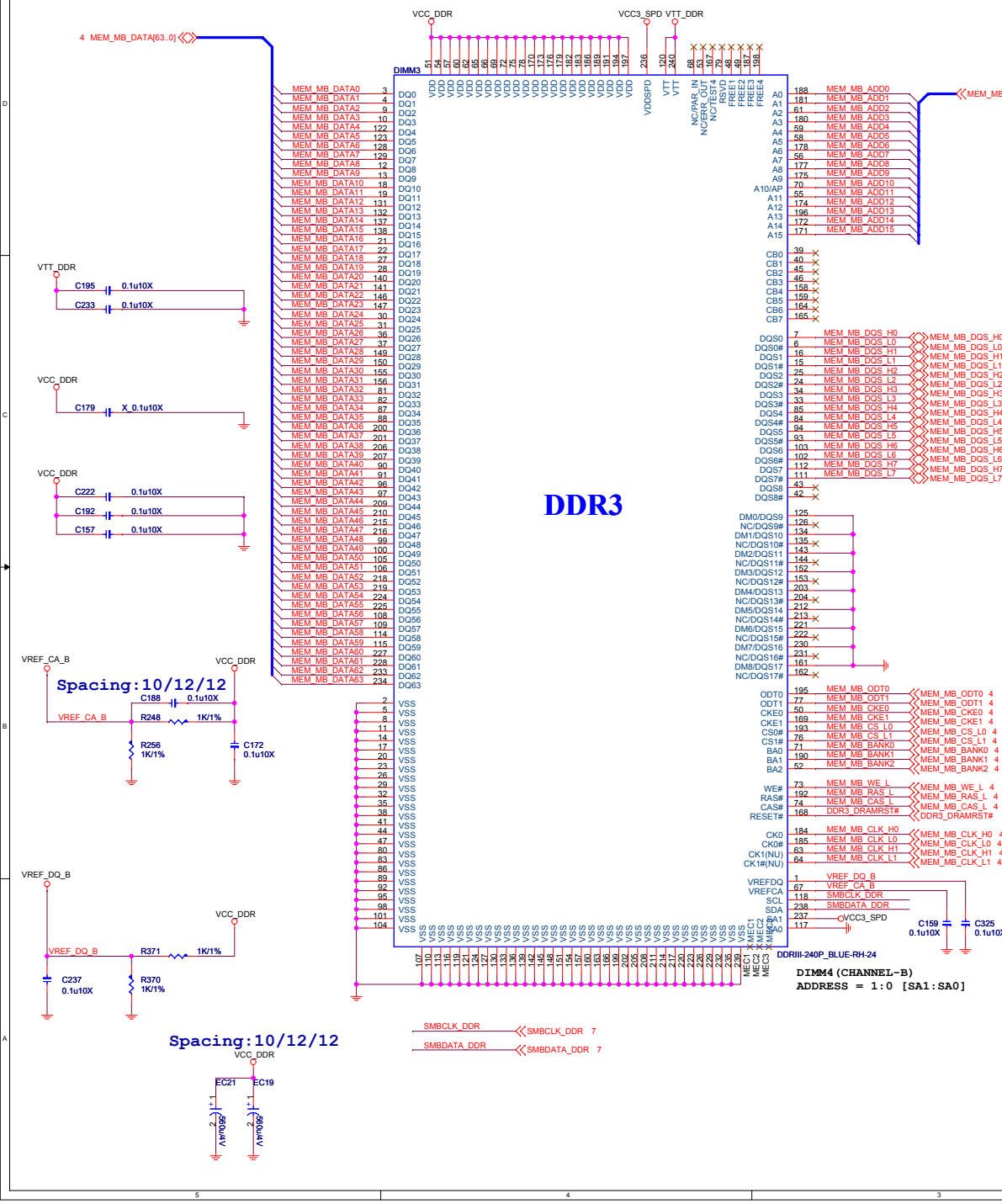
MICRO-STAR INT'L CO.,LTD

MS-7850

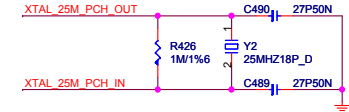
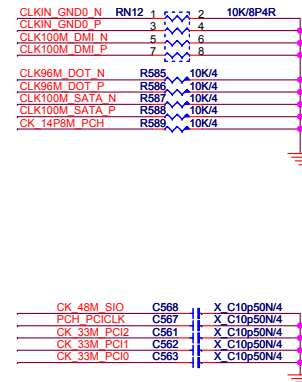
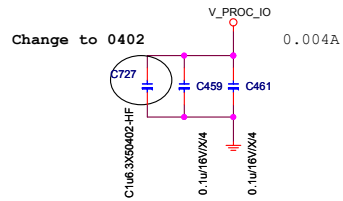
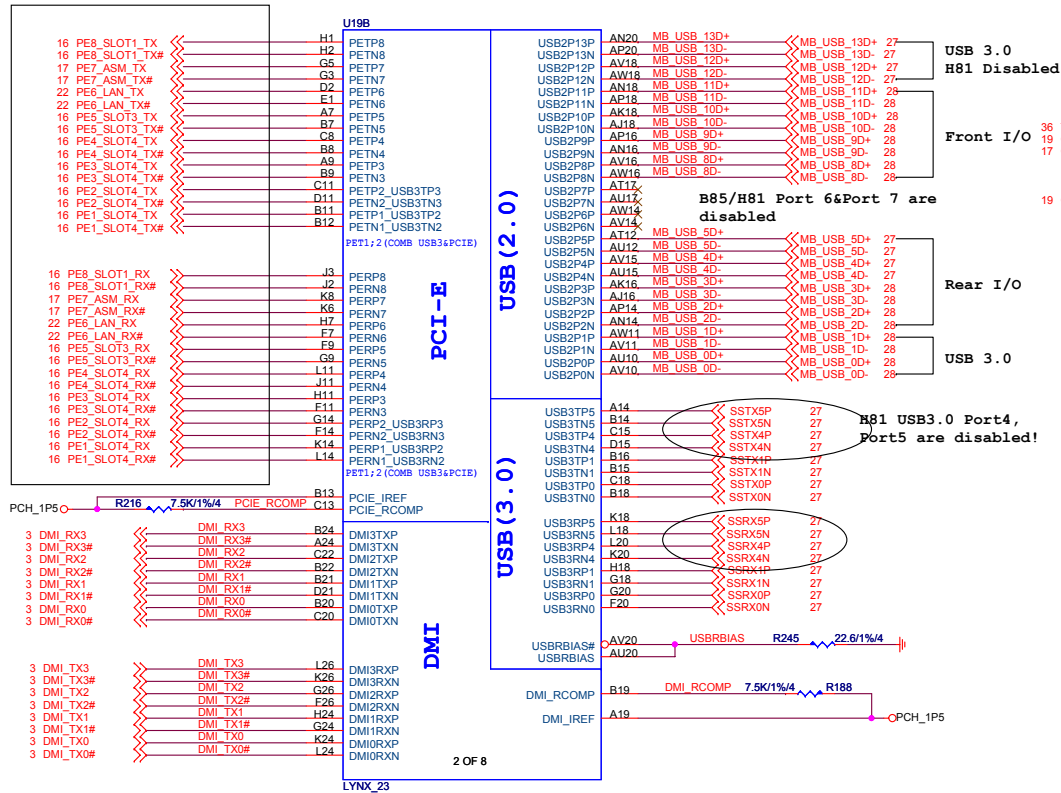
Size Custom Document Description DDR3 Chane-A DIMM1 Rev 0A Date: Thursday, March 21, 2013 Sheet 7 of 41

# DDRIII DIMM\_B0

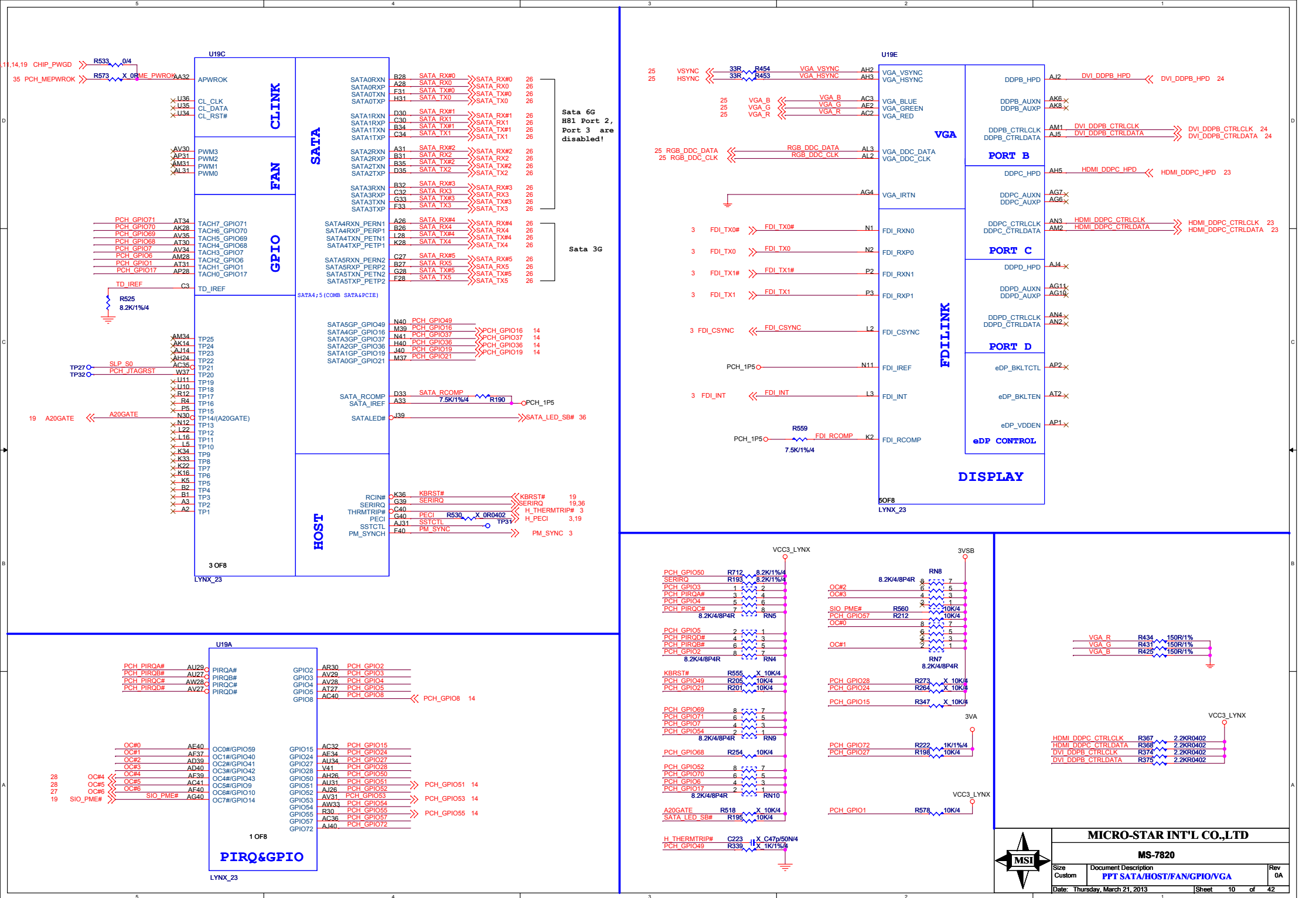
# DDRIII DIMM\_B1

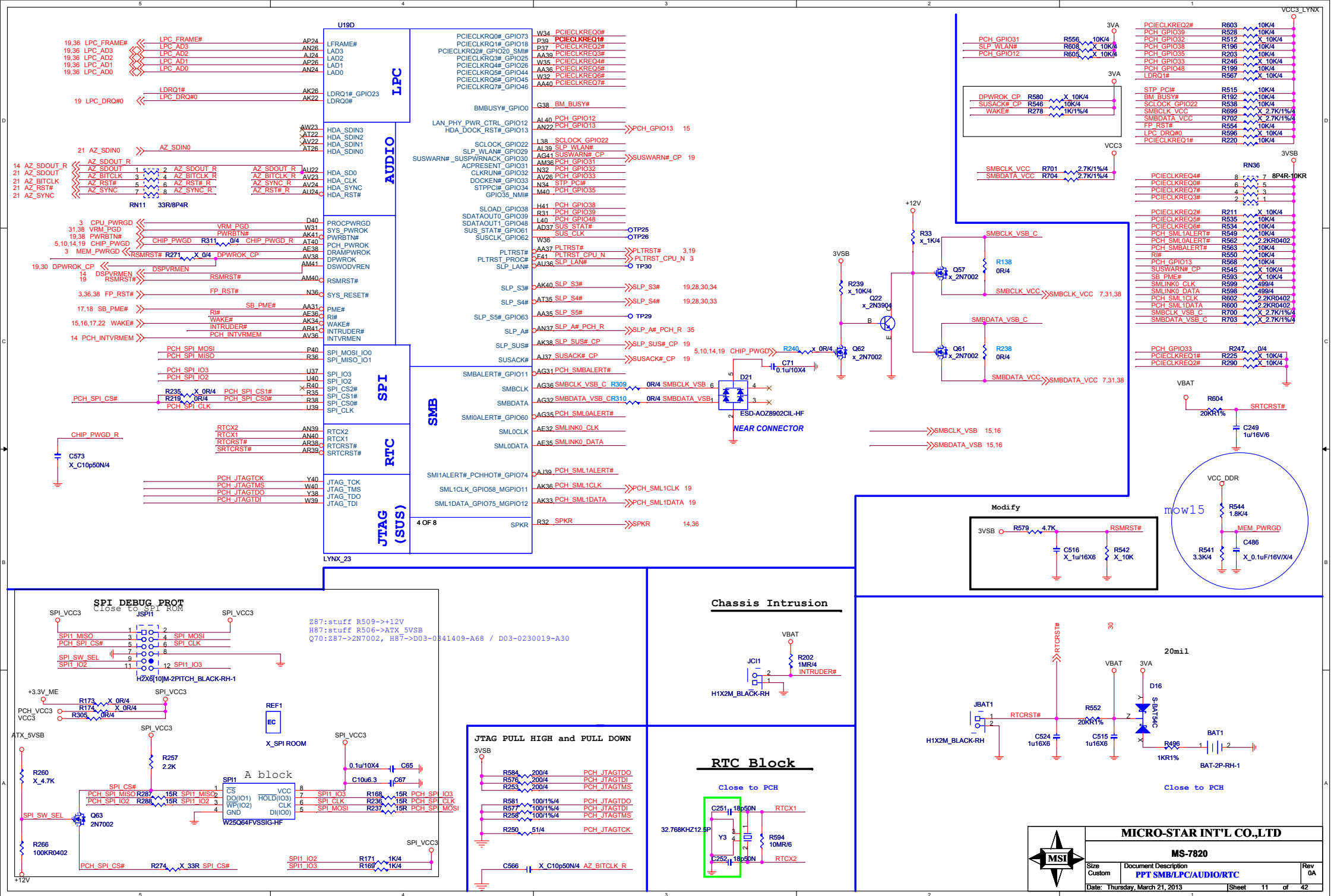






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MS-7820		
Size	Document Description	Rev
Custom	PPT PCIE/DMI/USB/CLK	0A
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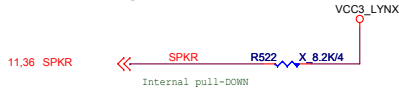
Pull high to enable integrated VRM



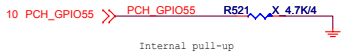
Pull high to enable integrated Deep-Sx well On-die VR



Internal weak pull down  
Pull high to enable "No Reboot" mode

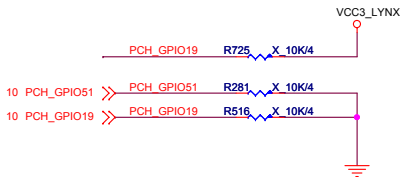


Internal weak pull up  
Pull low to enable "Top-Block Swap" mode



BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default



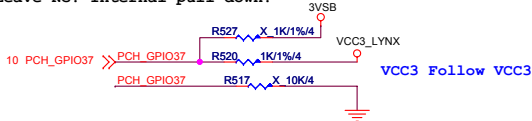
Do not pull low.  
Connect to ground with 1k Ohm pull-down resistor.



Enable TLS:

Pull up with 1k Ohm to VccSus3.3.  
Default (Disable TLS):

Leave NC. Internal pull down.

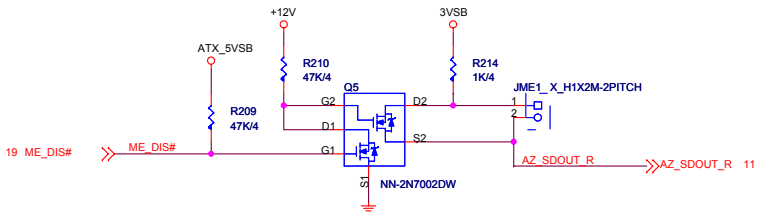


Default:

Do not pull high.

Disable ME in Manufacturing Mode:

Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.



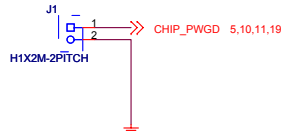
Internal weak pull down (function reserved)  
Signal should not be pulled high  
when strap is sampled



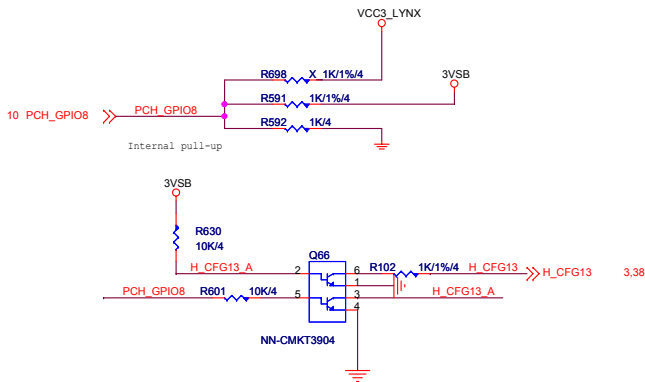
PCIE1 and SATA4 flexible IO function select  
High: SATA Low: PCIE



For test cpu voltage



Follow CRG 1.0



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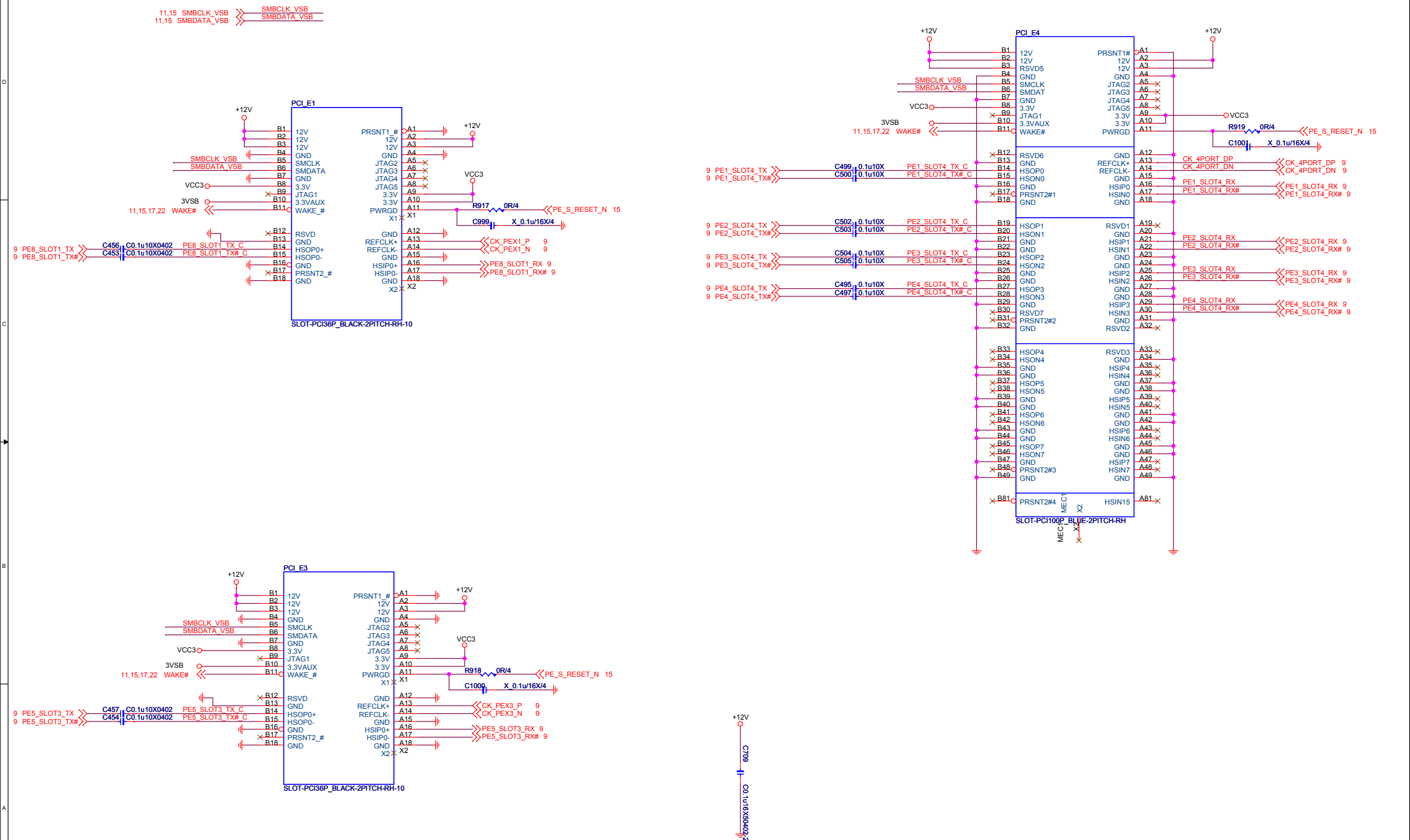
MS-7820

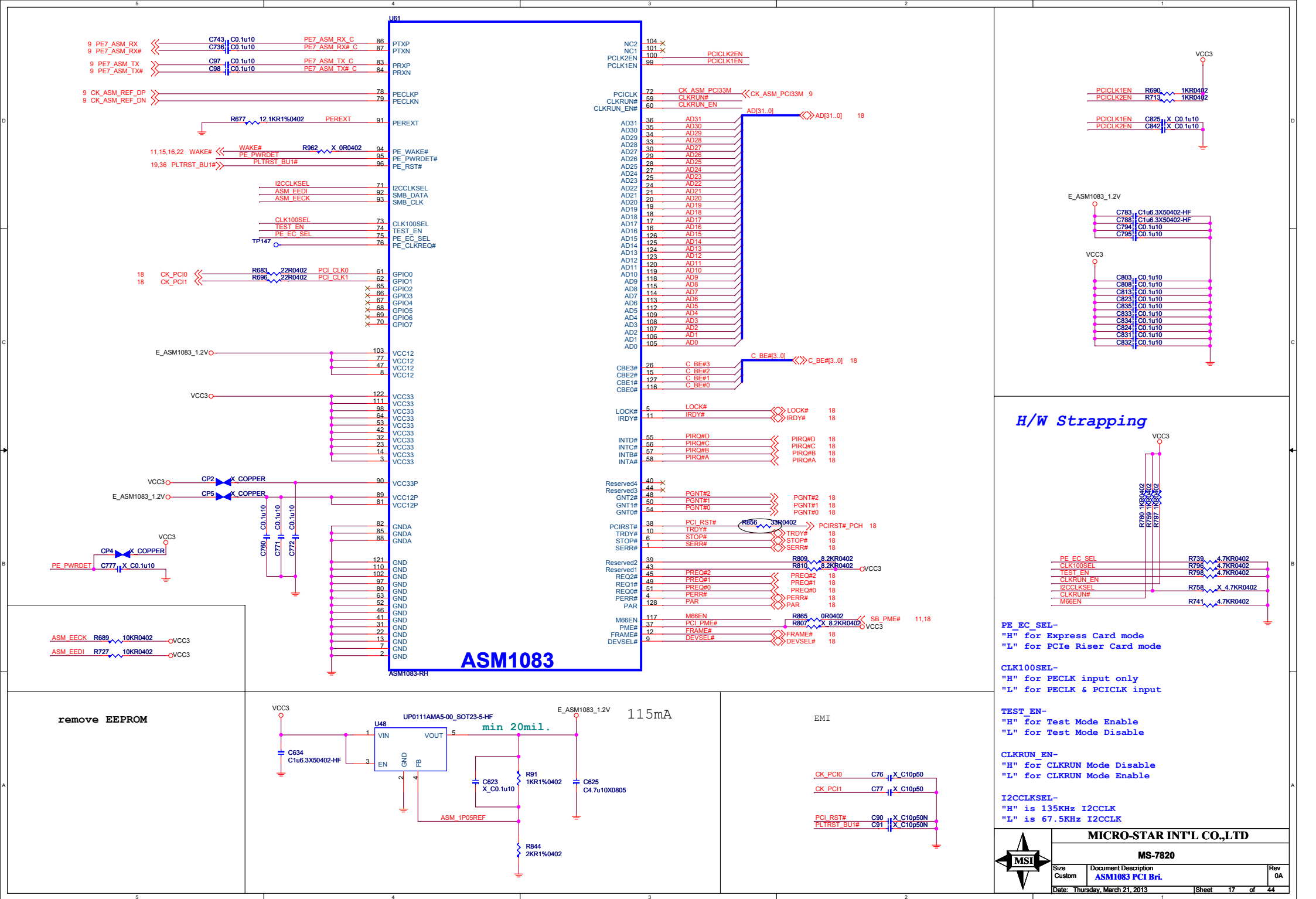
Size Custom	Document Description PPT STRAPS	Rev 0A
Date: Thursday, March 21, 2013	Sheet 14 of 42	



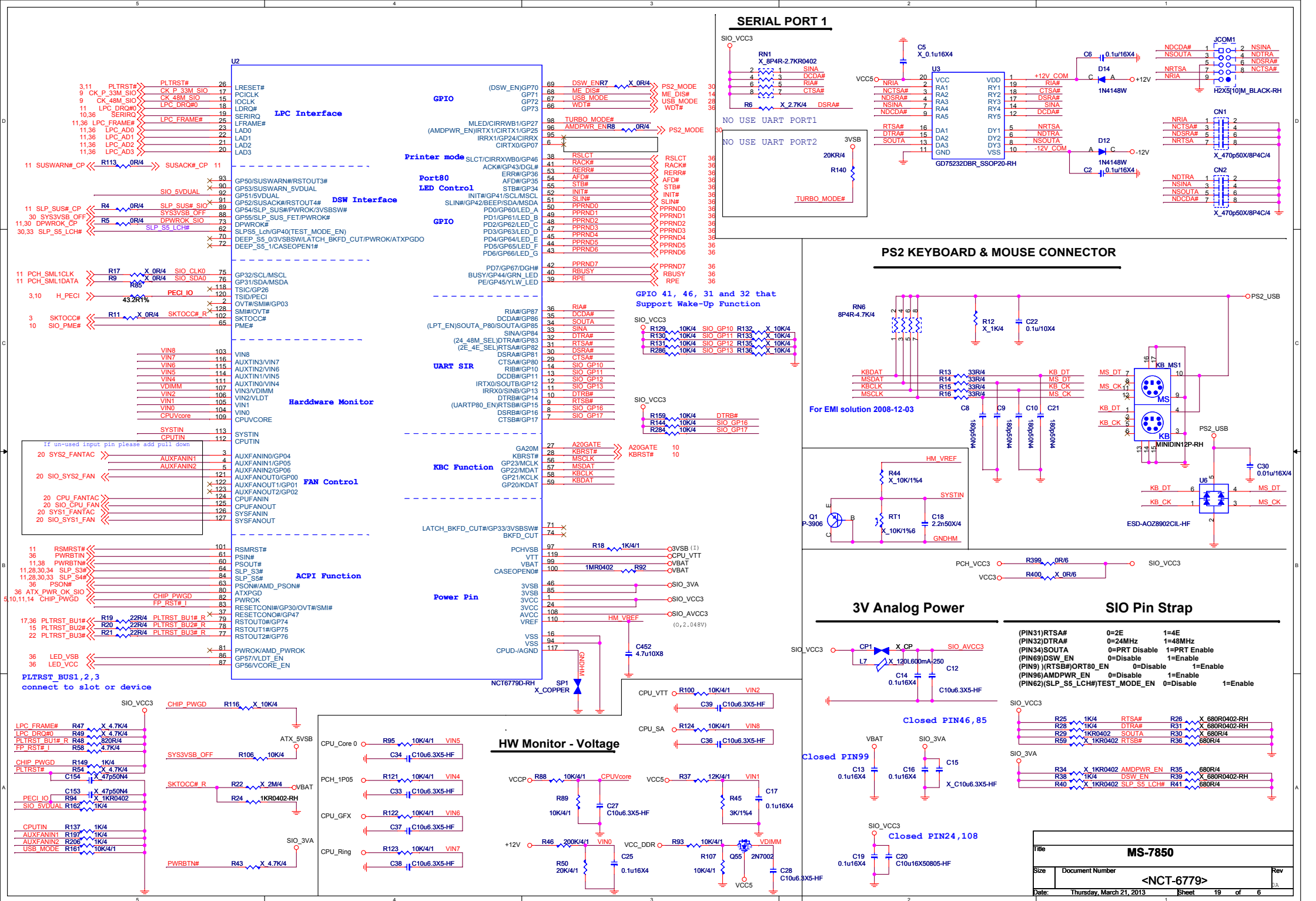


# PCI Express X4 Slot

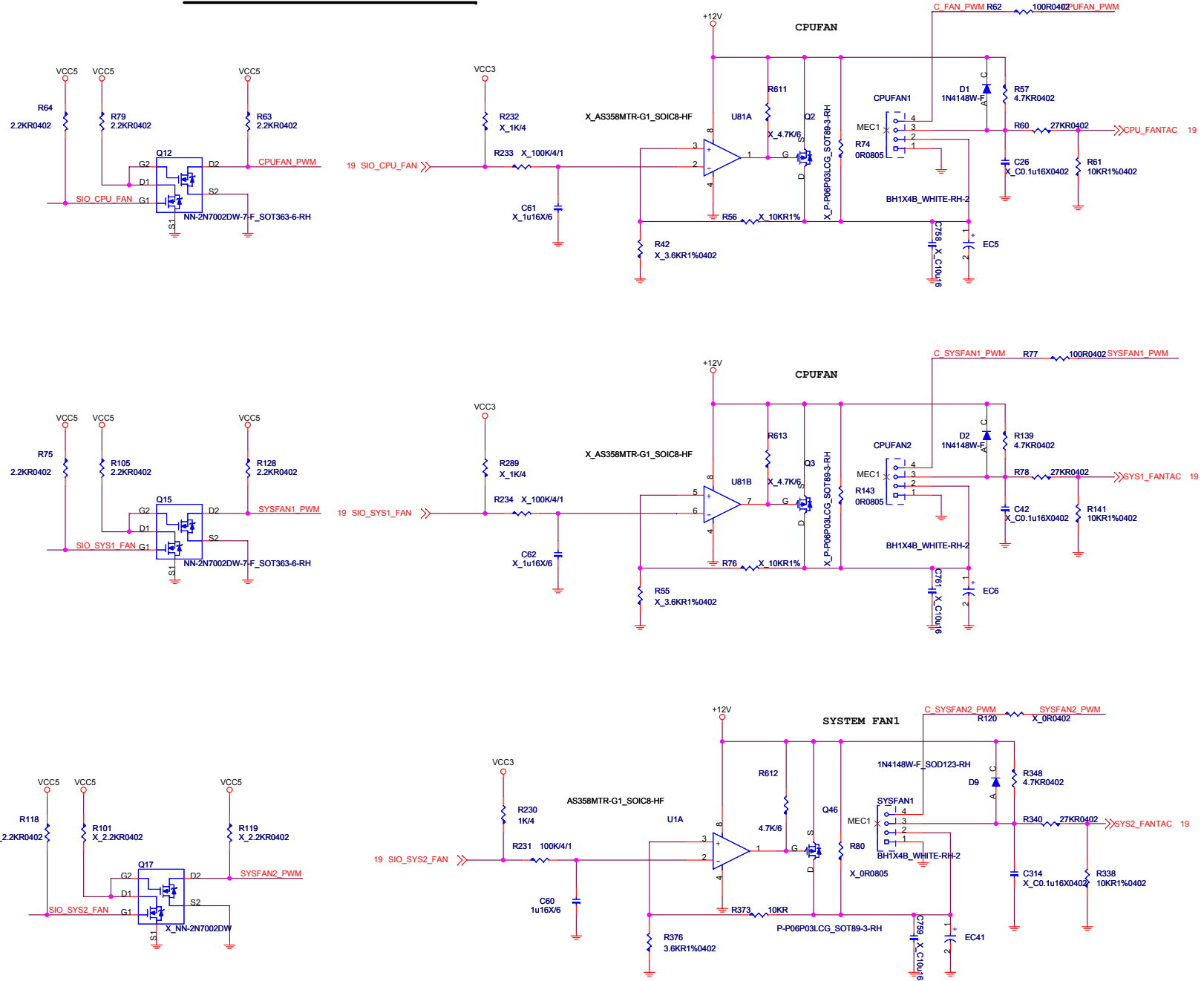








# FAN-COUNTROL CIRCUIT



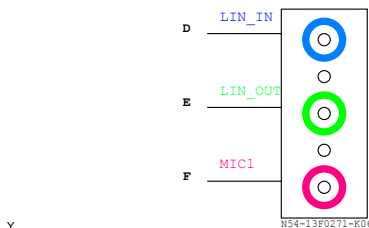
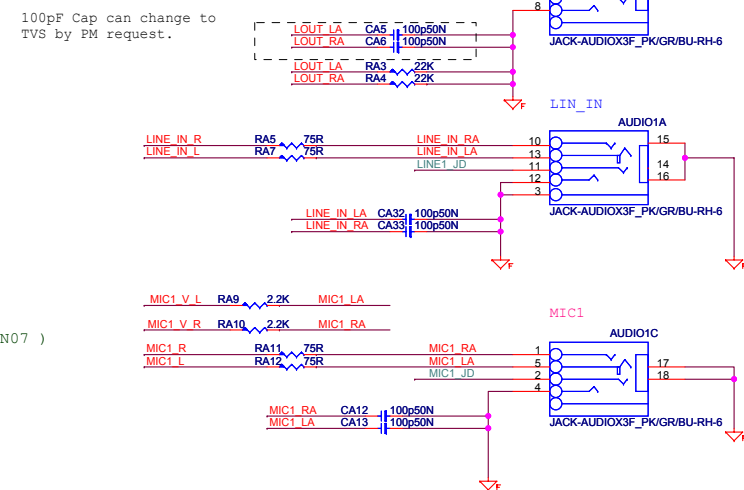
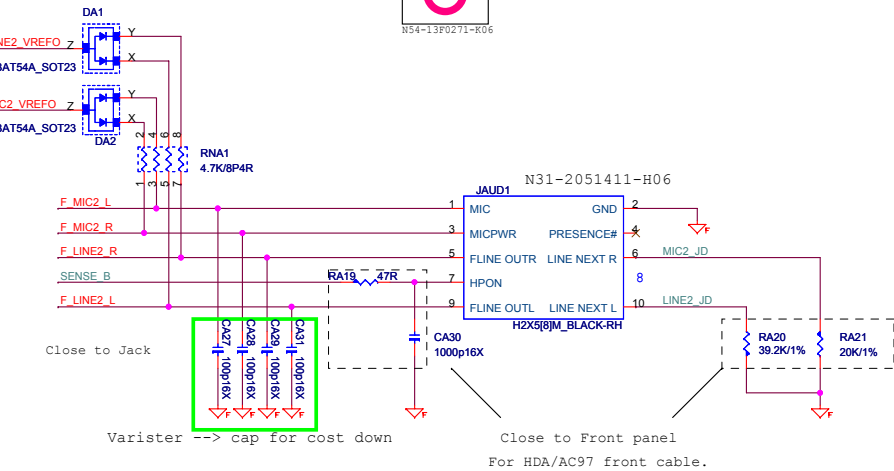
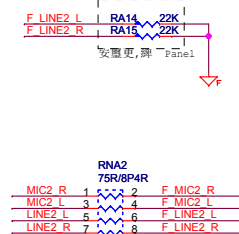
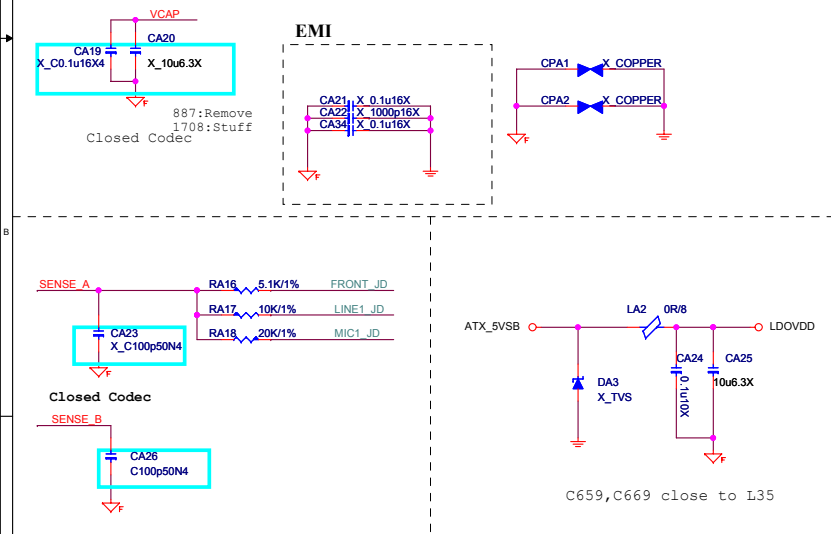
MICRO-STAR INT'L CO.,LTD

MS-7820

Size	Document Description	Rev
Custom	FAN Control	0A
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## VT1708S CE



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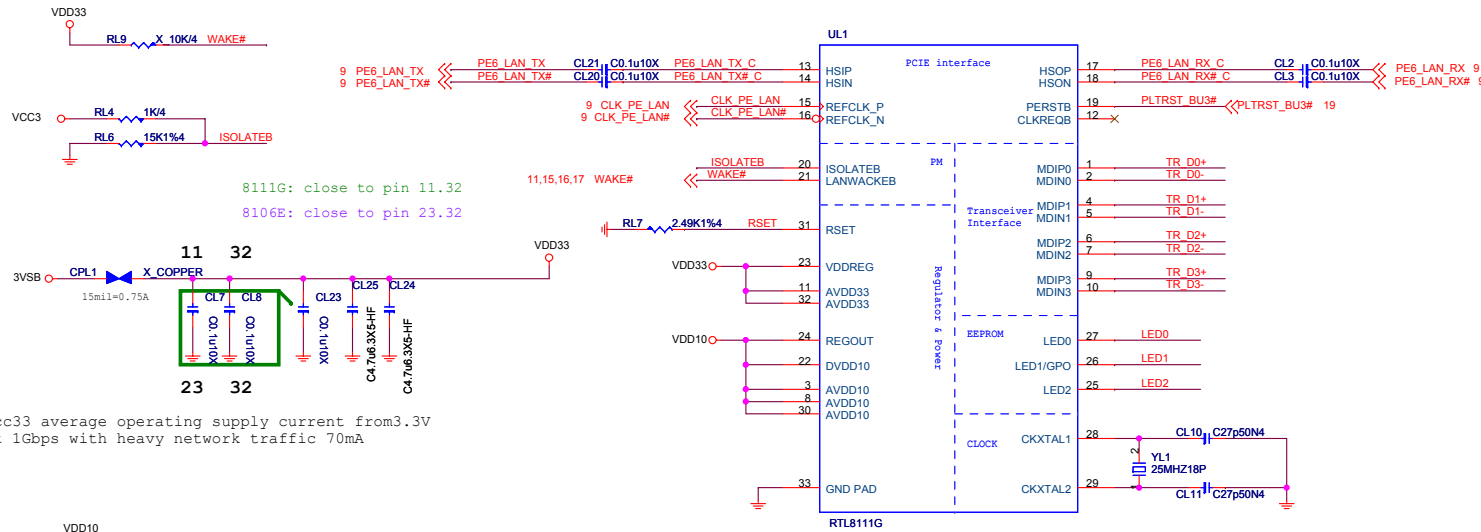
MS-7850

Size Custom	Document Description <b>Audio Codec ALC887</b>	Rev 0A
Date: Thursday, March 21, 2013		Sheet 21 of 41

# RTL8111G Giga LAN

## RTL8106E 10/100M LAN

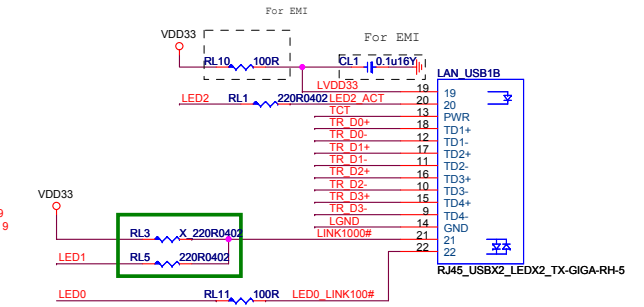
### LAN Connector



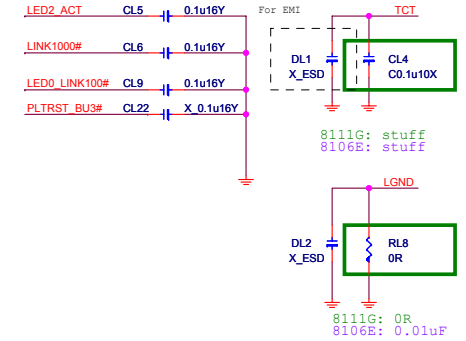
Icc33 average operating supply current from 3.3V  
At 1Gbps with heavy network traffic 70mA

8111G: close to pin 11.32  
8106E: close to pin 23.32

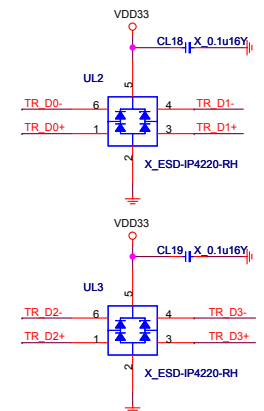
Icc10 average operating supply current from 1.0V  
At 1Gbps with heavy network traffic 300mA



8111G: Keep RL6 and Remove RL5 for RTL8111G  
8106E: Keep RL5 and Remove RL6 for RTL8106E



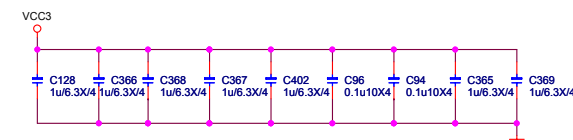
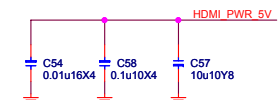
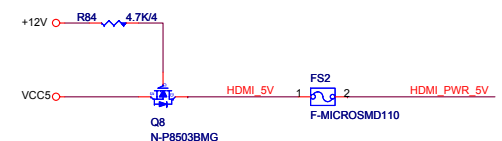
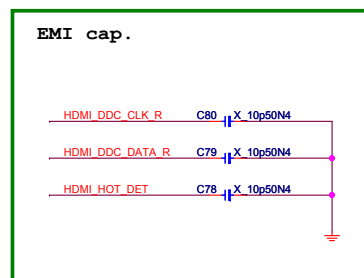
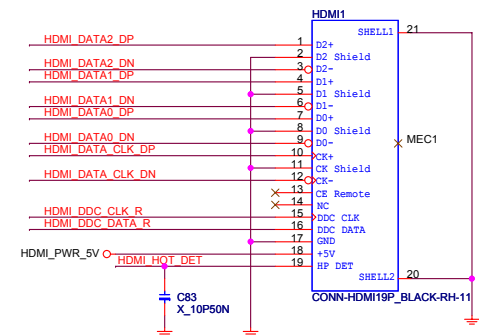
### Reserve ESD Protect



## HDMI level shifter

Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

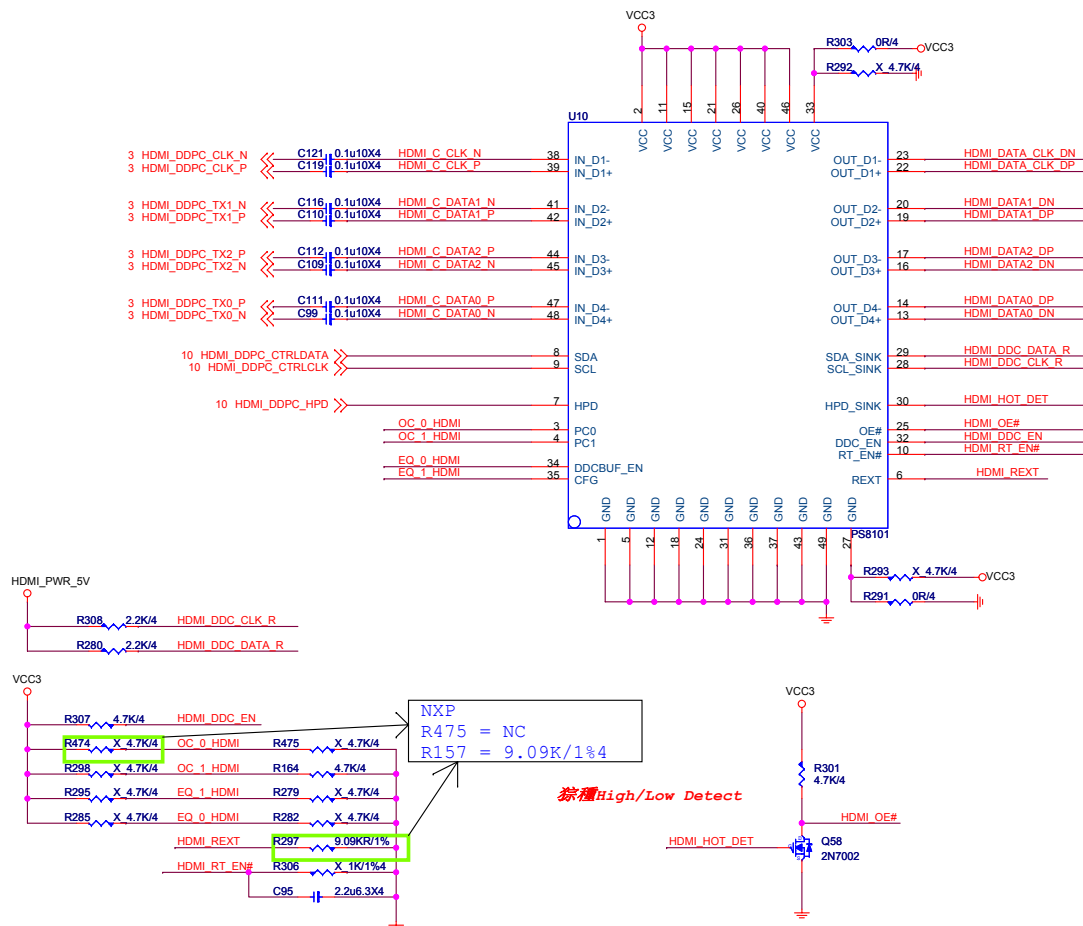
Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_ON
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_OP
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
SDVO_CTRLDATA	HDMIB_CTRL_DATA		



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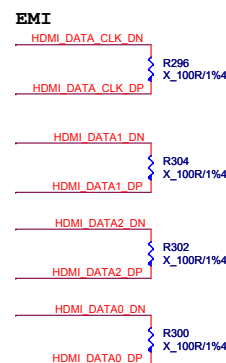
Size Custom	Document Description <b>HDMI Connector</b>	Rev 0.
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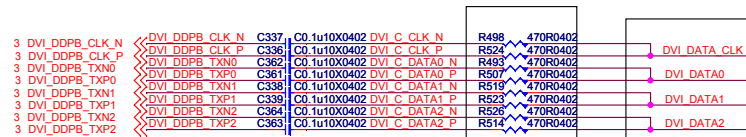
	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

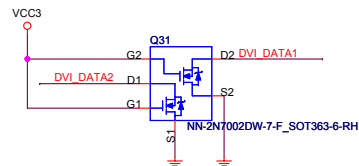
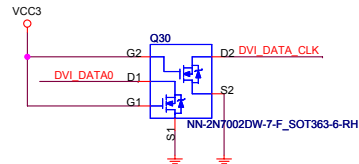
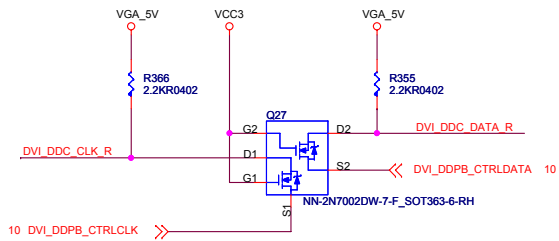
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	



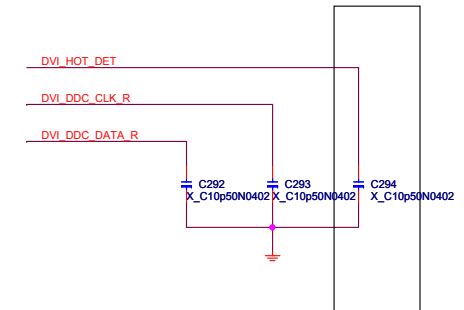
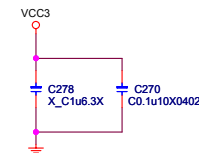
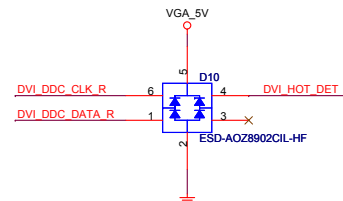
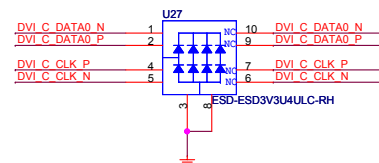
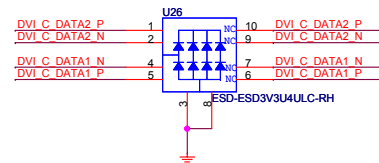
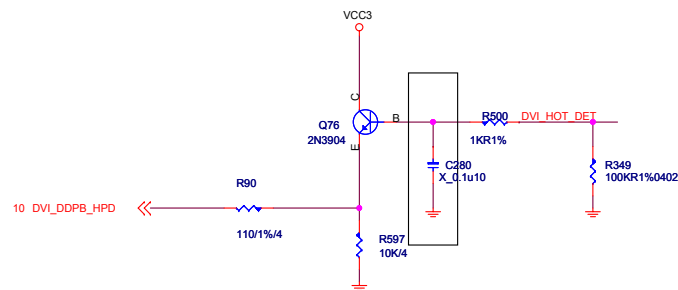
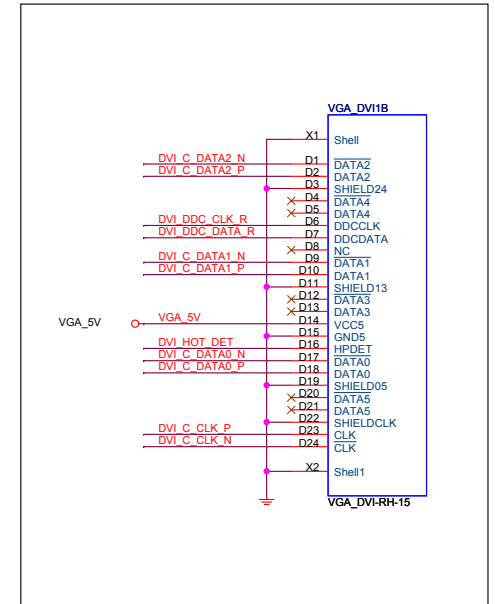
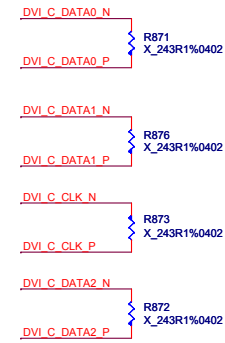
# VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



2013.03.19



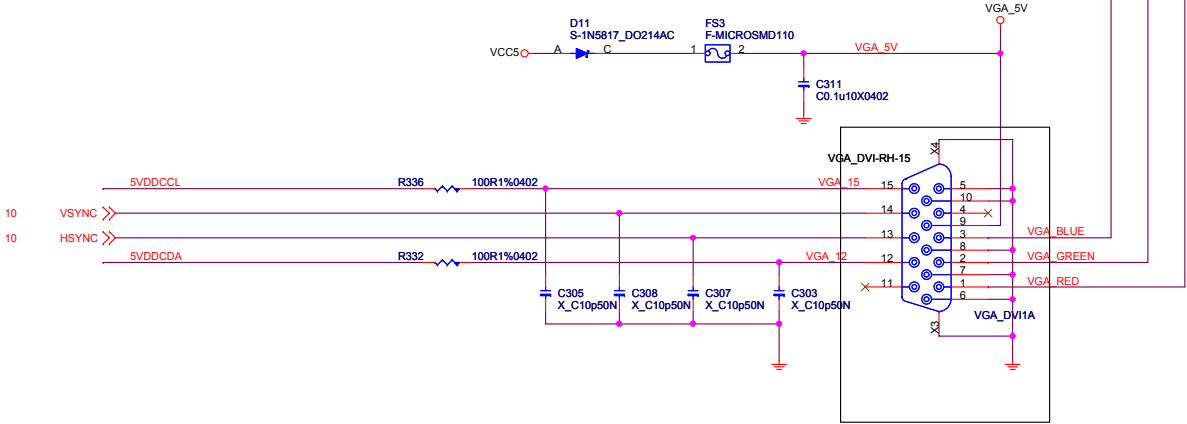
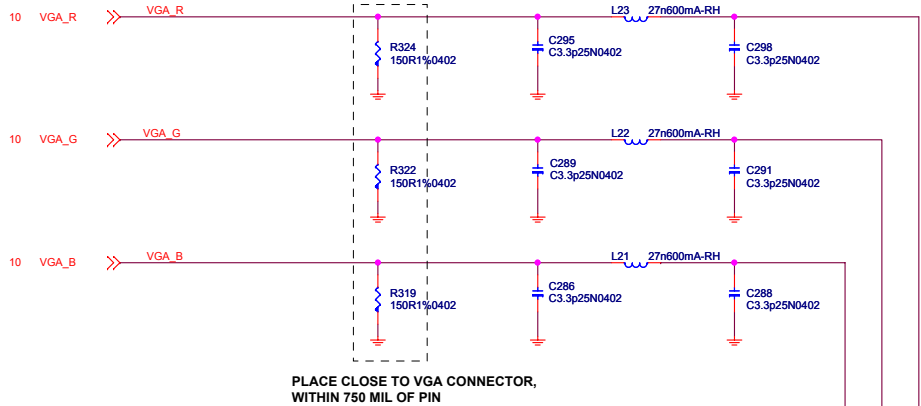
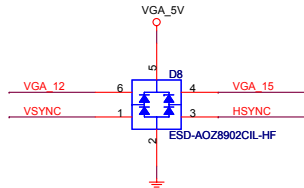
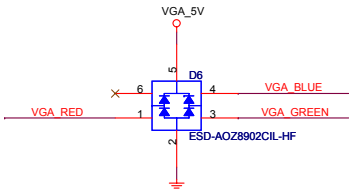
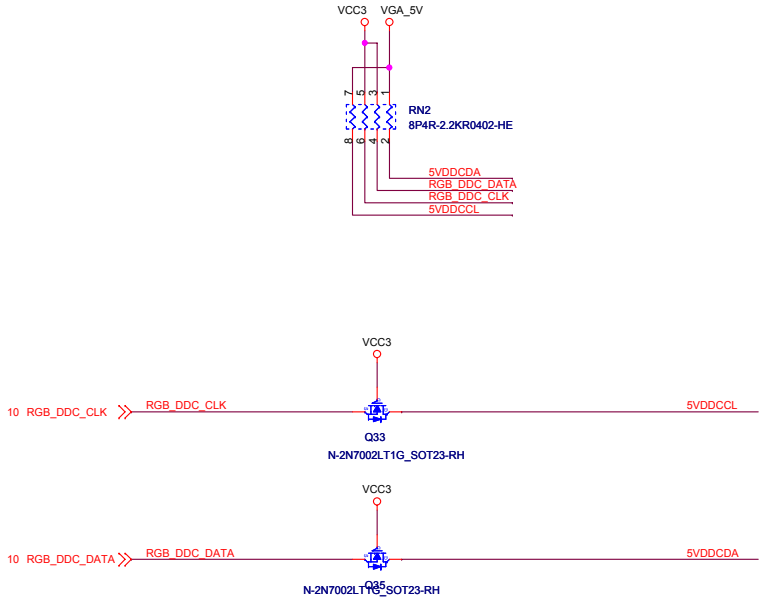
## For EMI



D-Sub

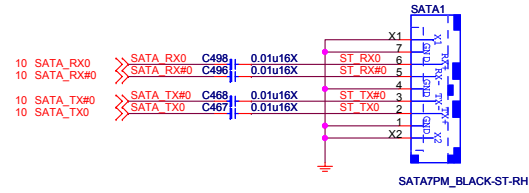
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Levelshift

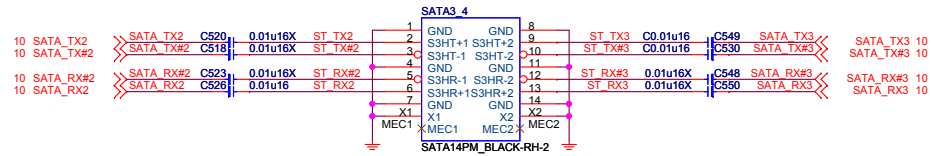


### SATA 6G PORT 0,1

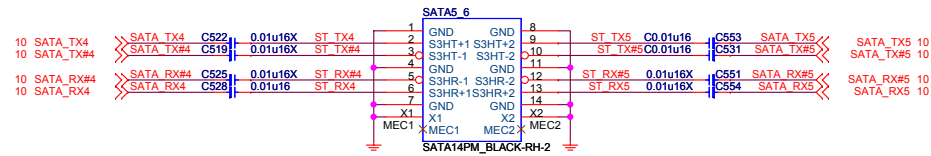
3.0 white



### SATA 6G PORT 2,3



### SATA 6G PORT 4,5

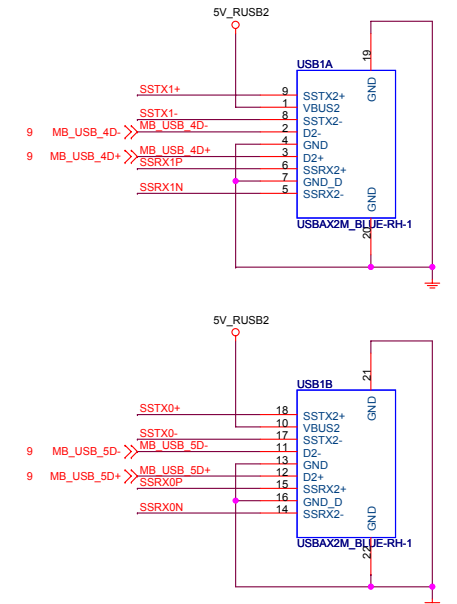
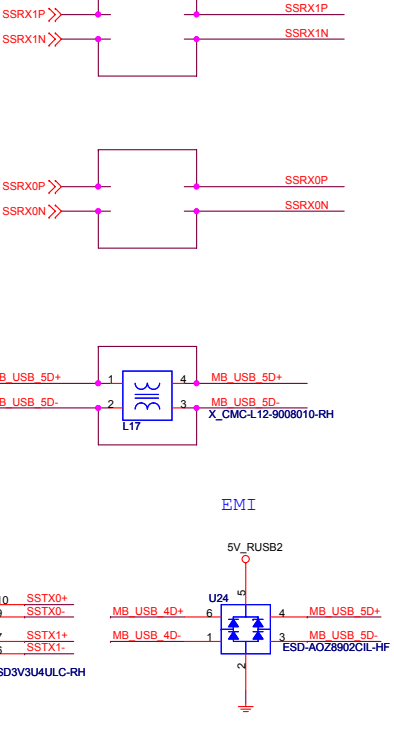
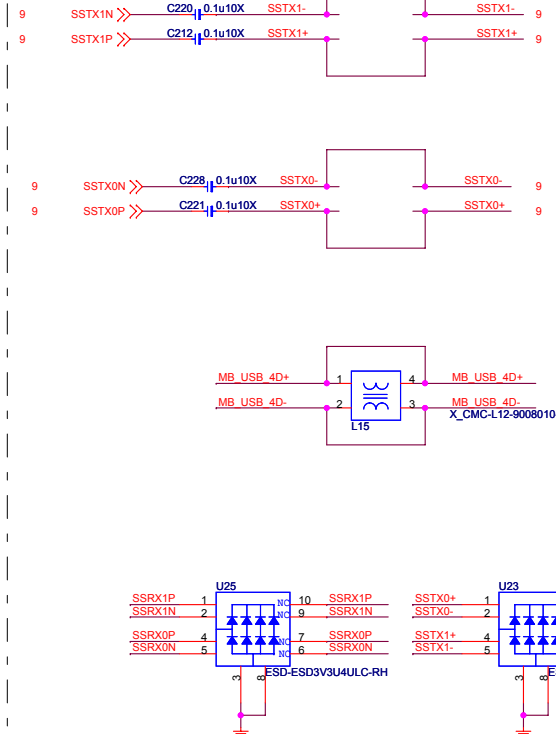
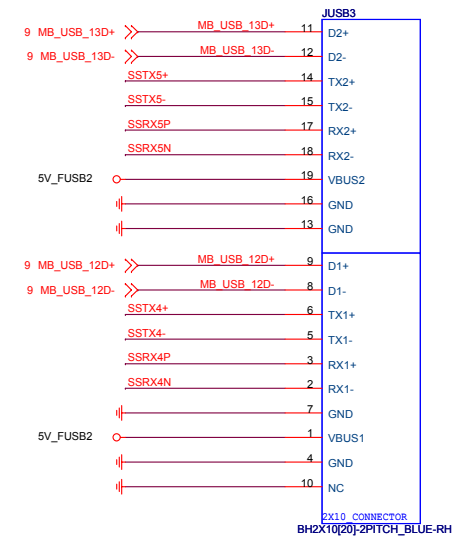
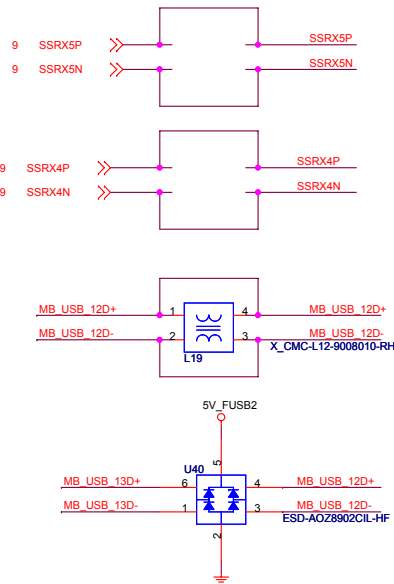
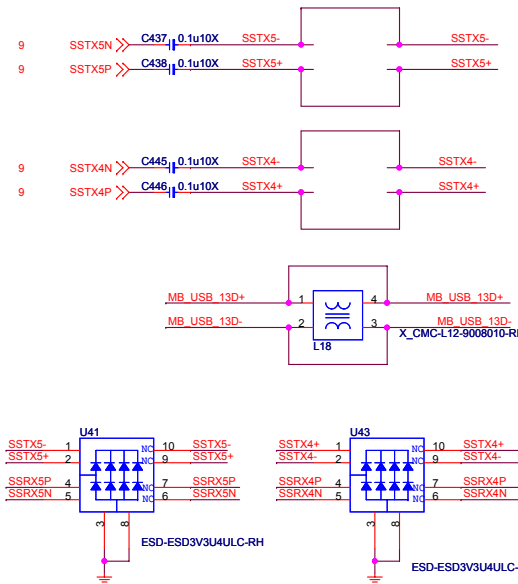
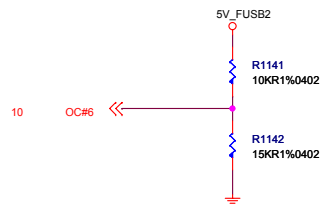


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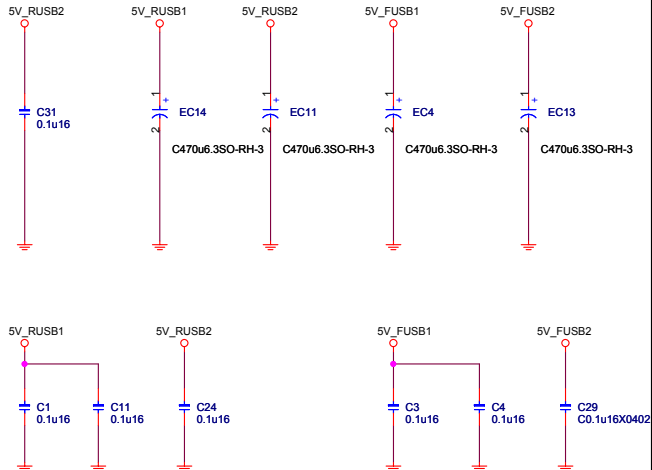
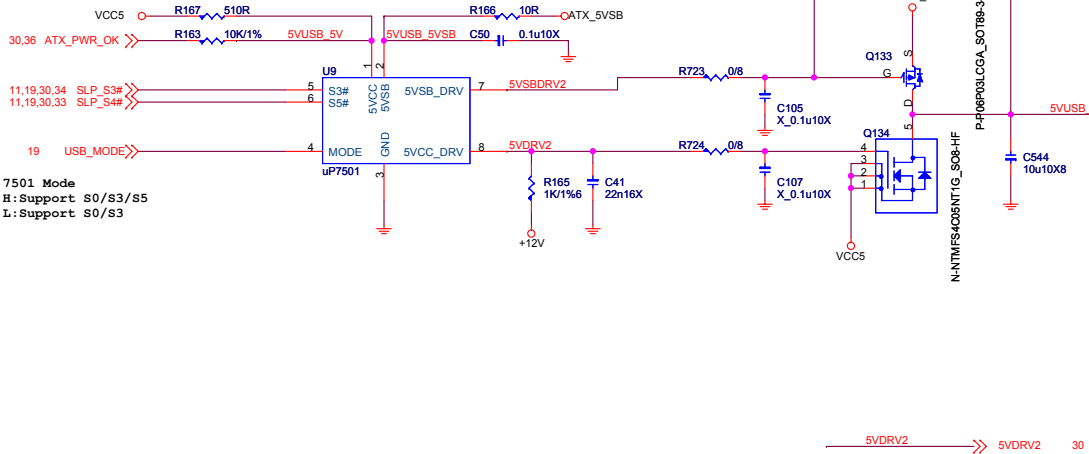
Size	Document Description	Rev
Custom	SATA Connector	0A
Date: Thursday, March 21, 2013		
Sheet 26 of 44		



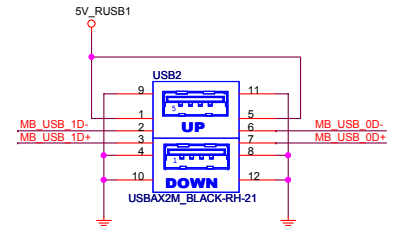
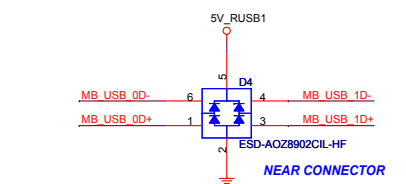
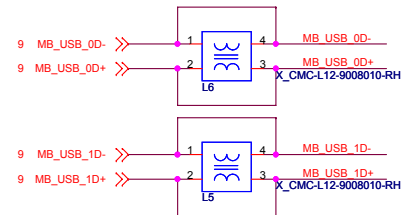


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Size Custom	Document Description <b>USB3.0 Connector</b>	Rev 0A
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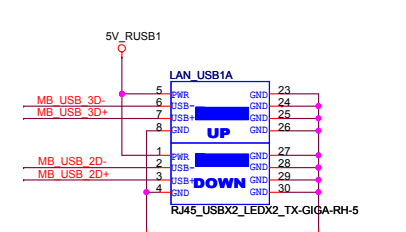
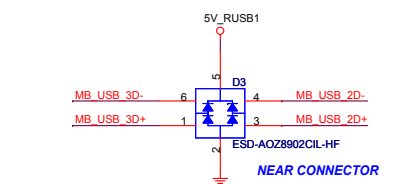
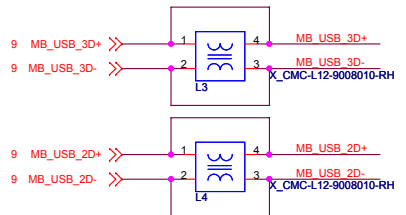
USB2.0/PS2 POWER Control  
**5VDIMM FOR DDR**



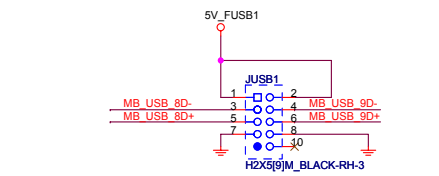
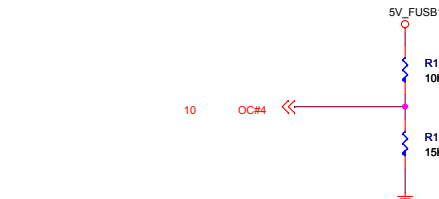
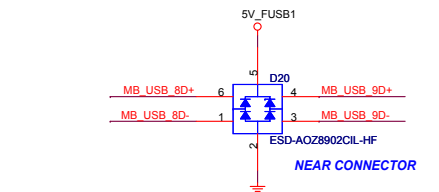
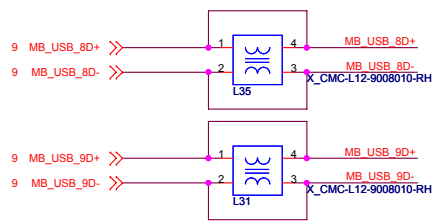
**FRONT USB PORT2,3**



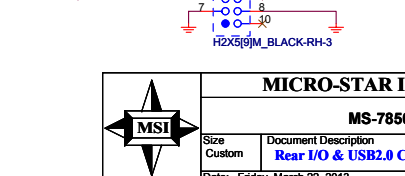
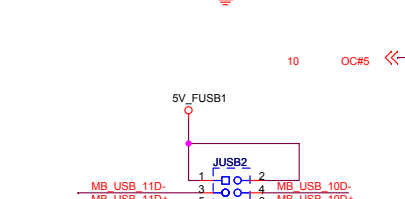
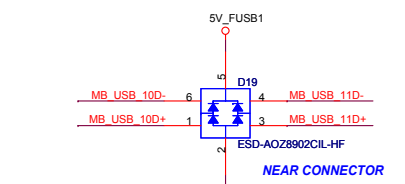
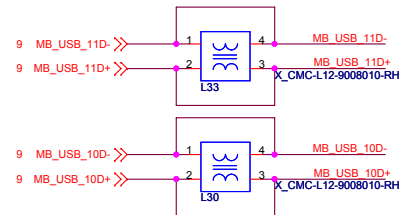
**FRONT USB PORT4,5(With Lan)**




**FRONT USB PORT8,9**



**FRONT USB PORT 10,11**

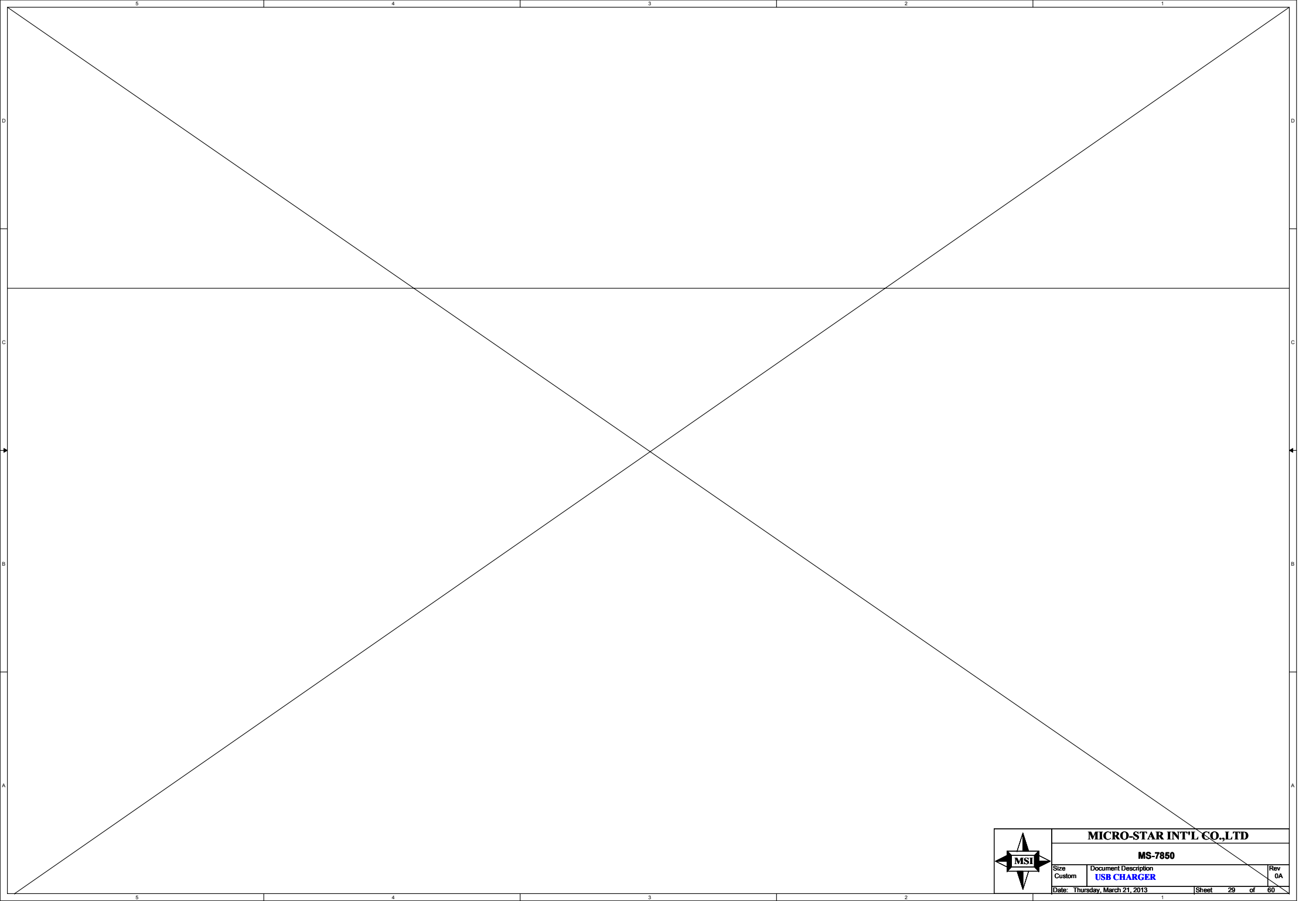





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**MS-7850**

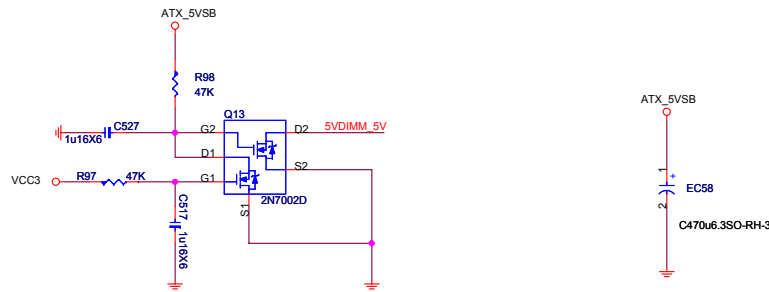
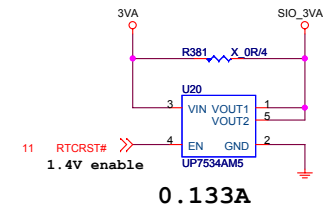
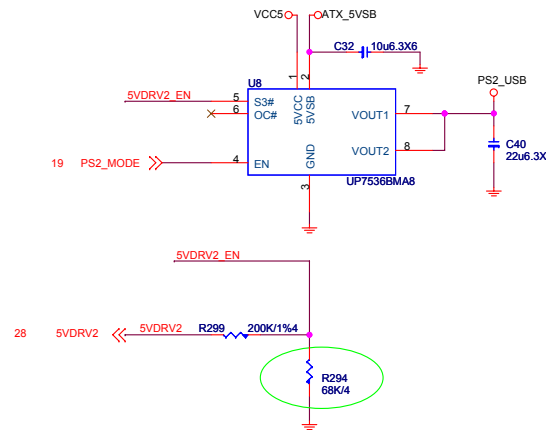
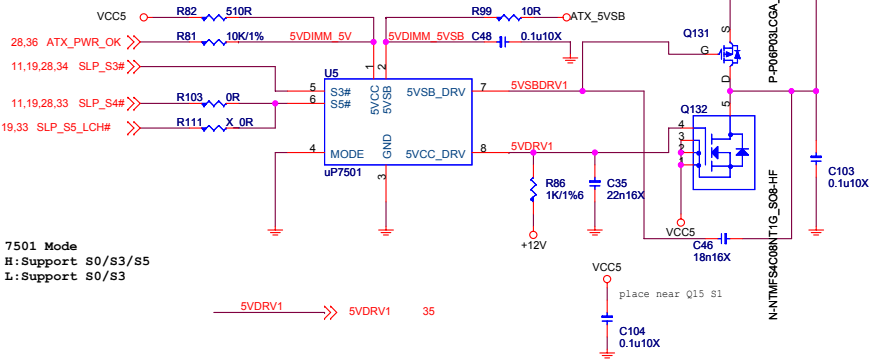
Size	Document Description	Rev
Custom	Rear I/O & USB2.0 Connector	0A
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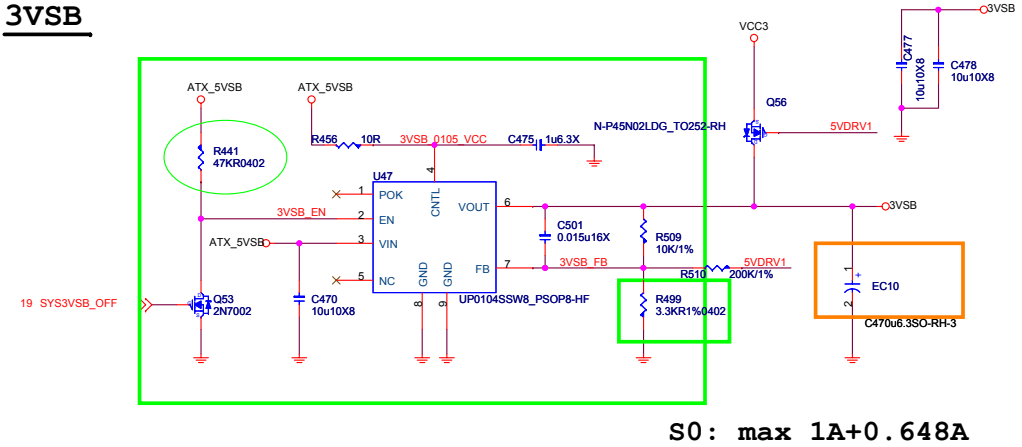


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Size Custom	Document Description <b>USB CHARGER</b>	Rev 0A
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## 5VDIMM FOR DDR

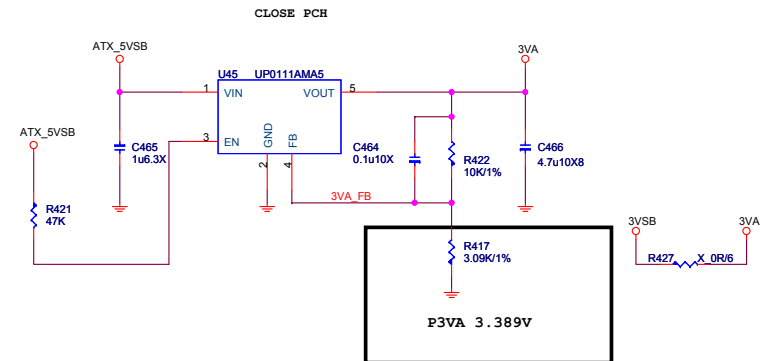


## 3VSB



## 3VA

20mA

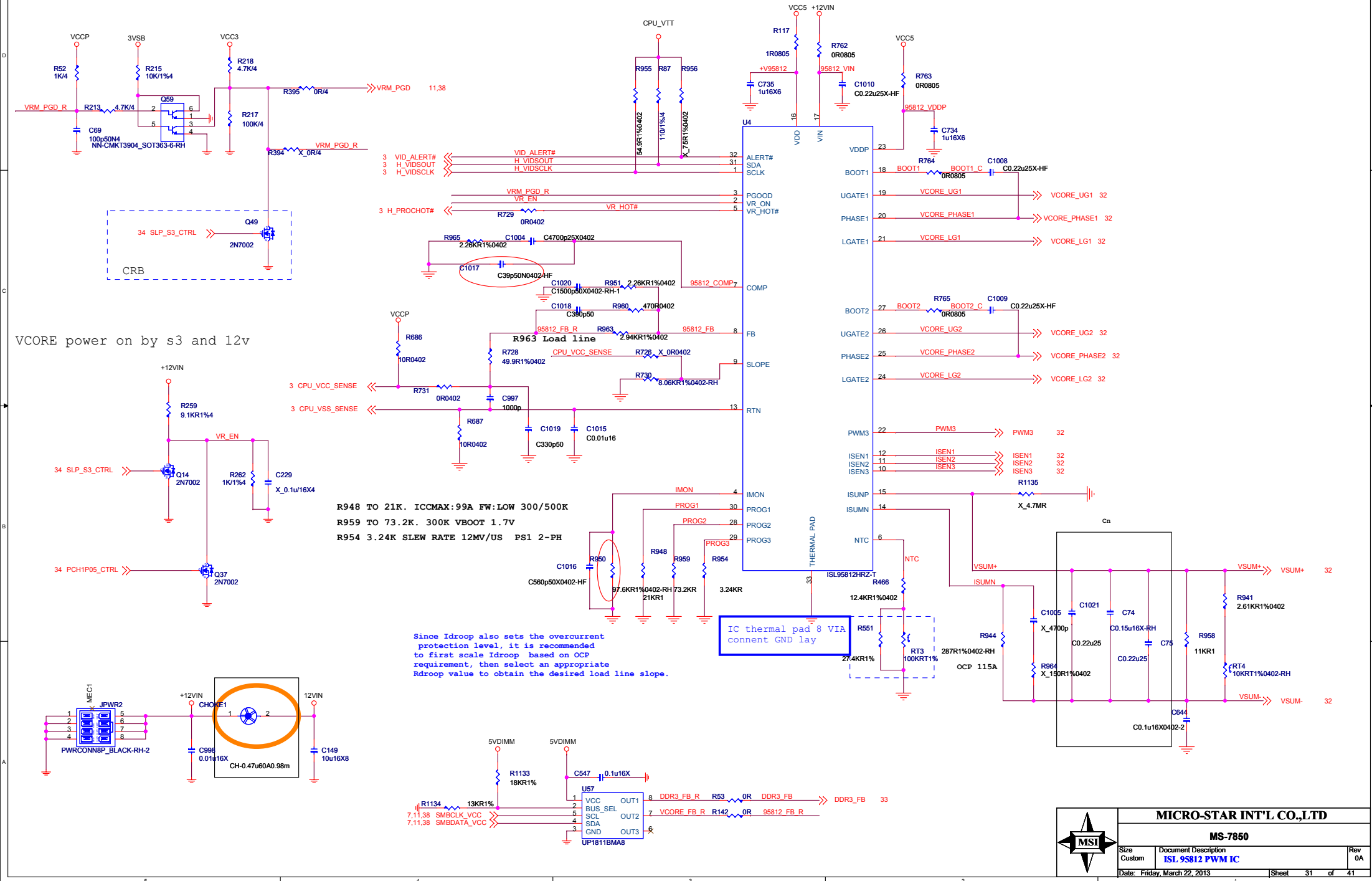


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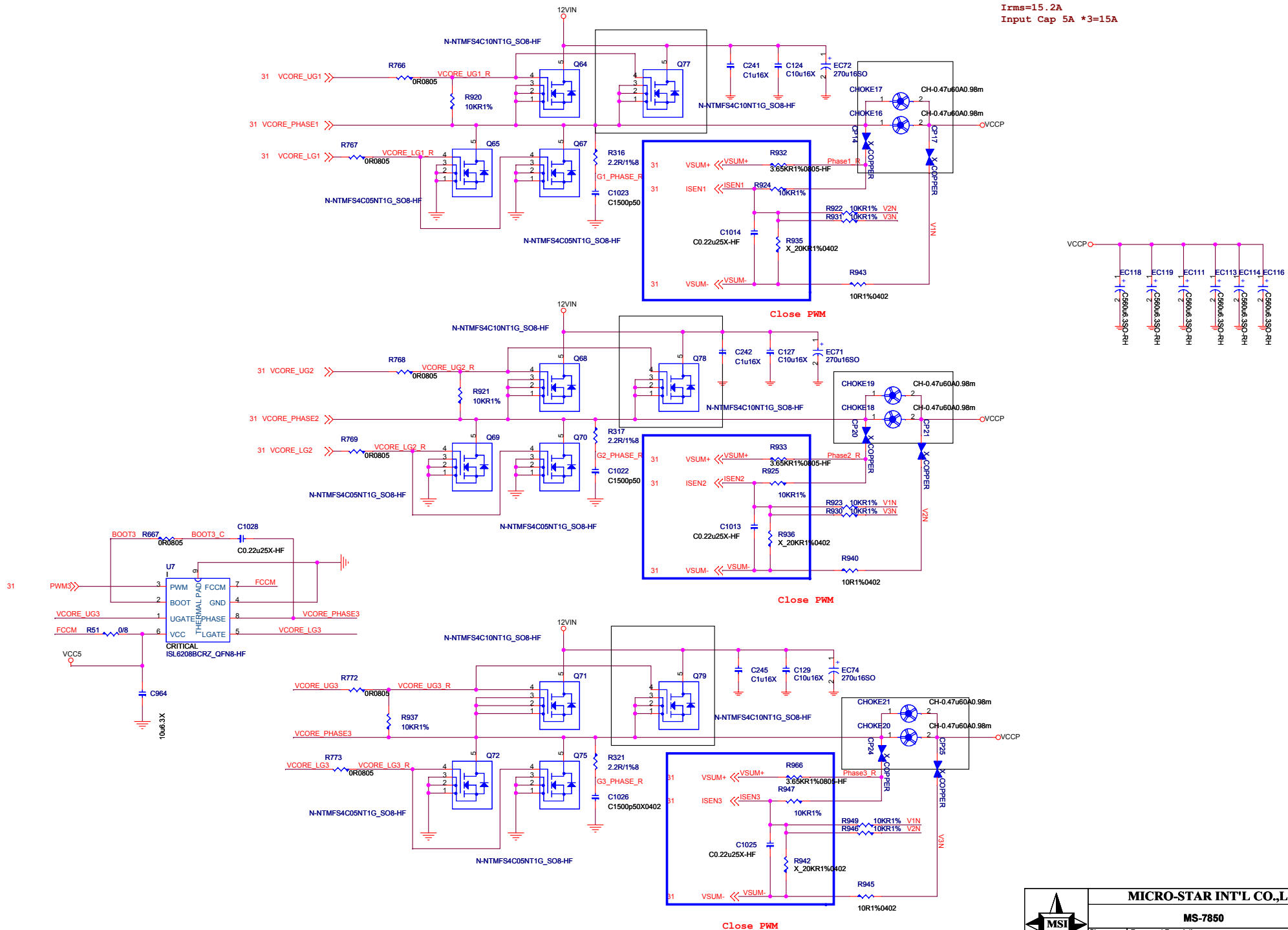
Size	Document Description	Rev
Custom	ACPI Power	0A
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ISL95812 FOR VR12.5 suggest  
schematic

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Size Custom	Document Description <b>ISL 95812 PWM IC</b>	Rev 0A
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OUTPUT CURRENT: ICCMAX 95A  
I<sub>rms</sub>=15.2A  
Input Cap 5A \*3=15A



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# DDR Power:1.5V

DDR3\_1.5V ICCMAX 24A

4.5A FOR CPU

12A FOR 4DIMM

1.1A FOR DDR VTT

6A FOR DDR PCH

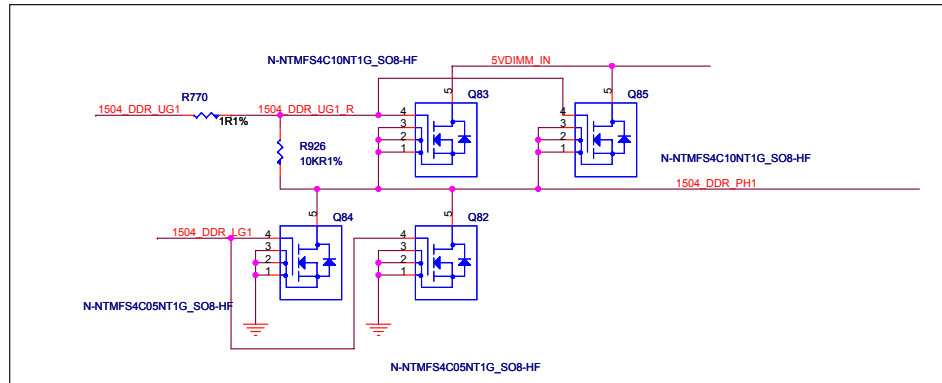
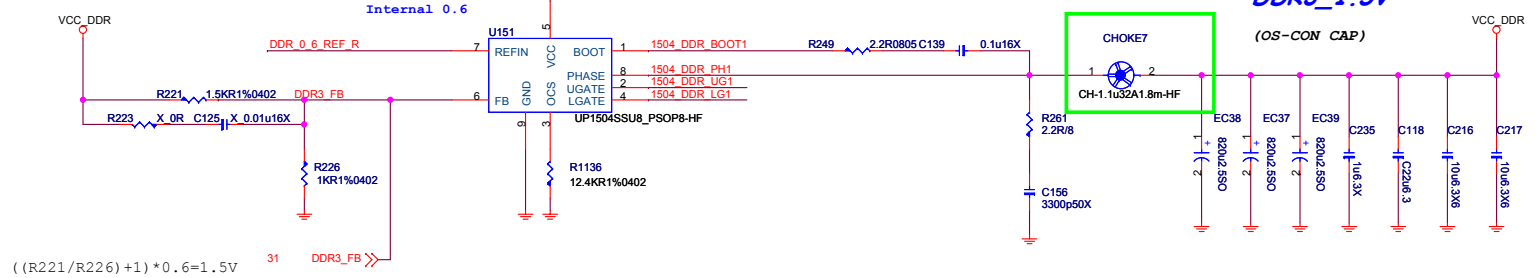
Tripple=9.6

4.7\*2\*1=9.4A<9.6A

OCP 24\*1.5=36A

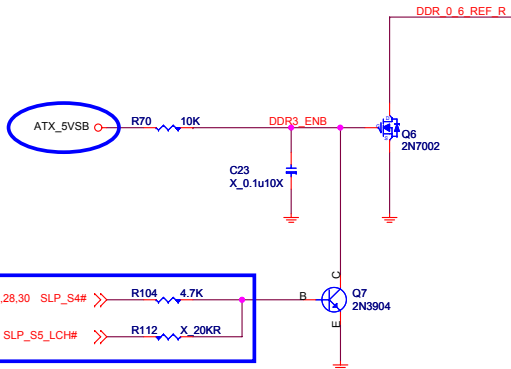
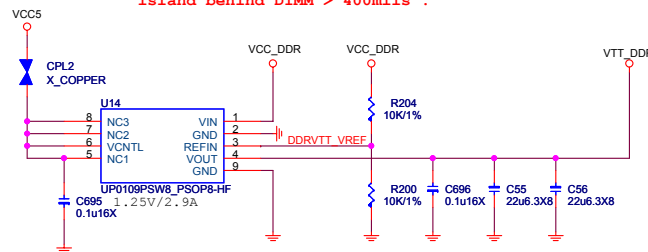
36A=20uA\*Rocs/4\*Rdson(Low side 1.7mohm)

Rocs=12.4K ohm



## DDR VTT Power

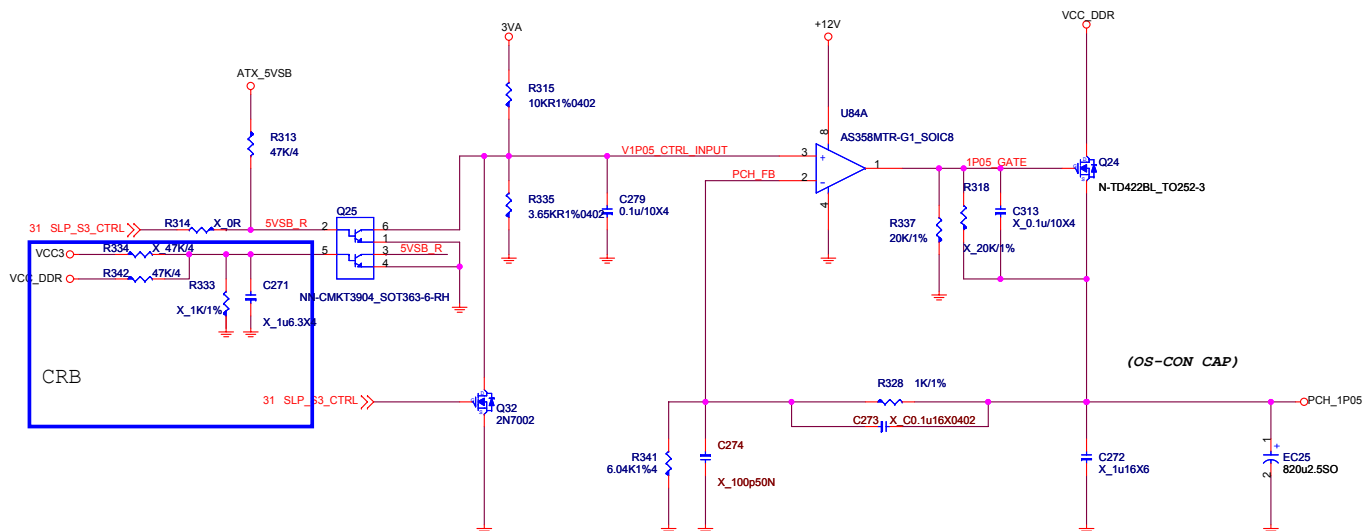
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



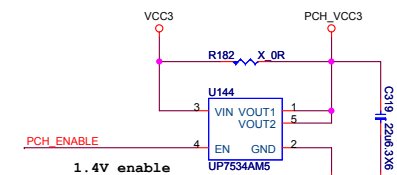
P.S. Only for meet Intel power down sequence.

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Size	Document Description	Rev	
Custom	DDR Power-UP1513 UP1504S	0A	
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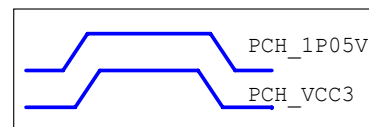
**PCH Power:1.05V 5.747A**



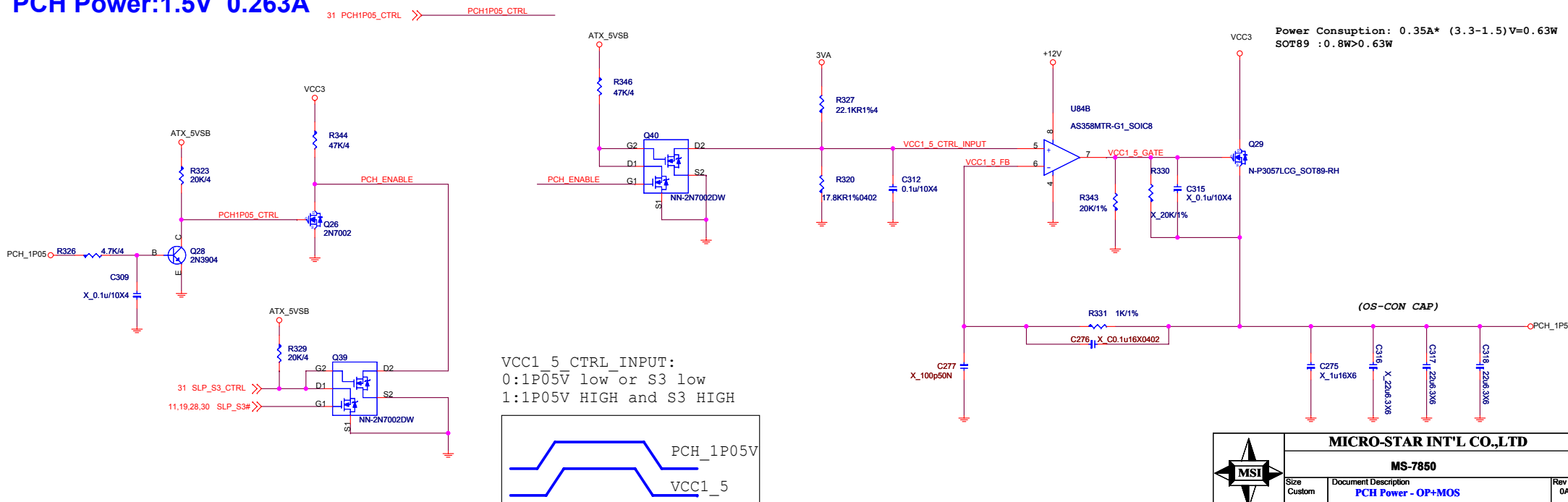
0.133A



```
VCC1_5_CTRL_INPUT:
0:1P05V low or S3 low
1:1P05V HIGH and S3 HIGH
```



**PCH Power:1.5V 0.263A**



**MICRO-STAR INT'L CO.,LTD**

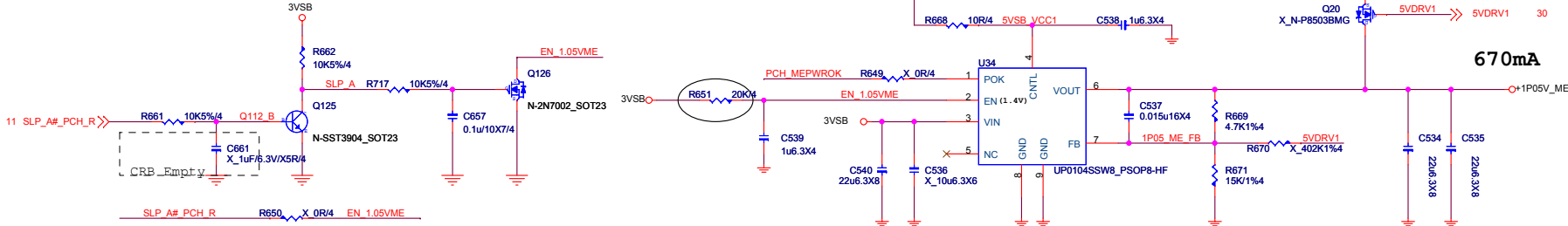
**MS-7850**

Size Custom	Document Description <b>PCH Power - OP+MOS</b>	Rev 0A
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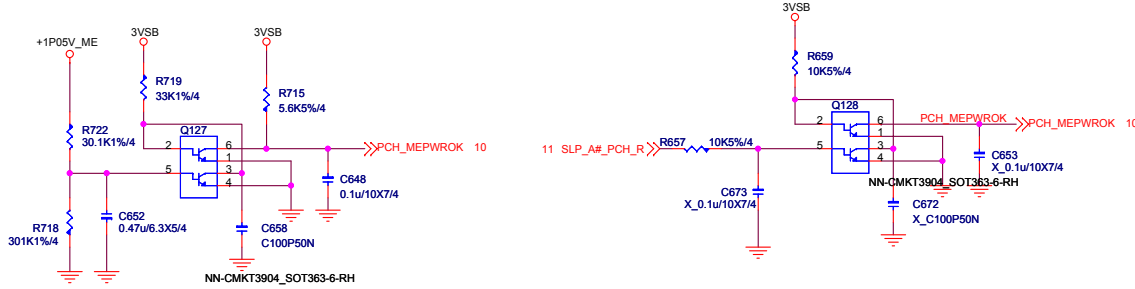
**+1.05V\_ME(VCCIO\_ME)**

SLP\_A

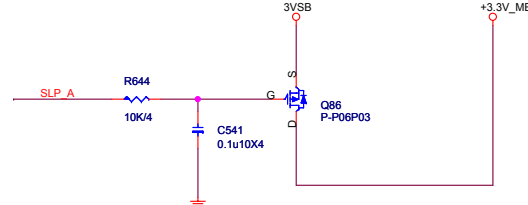
## ME Power Contro



PCH\_MEPWROK

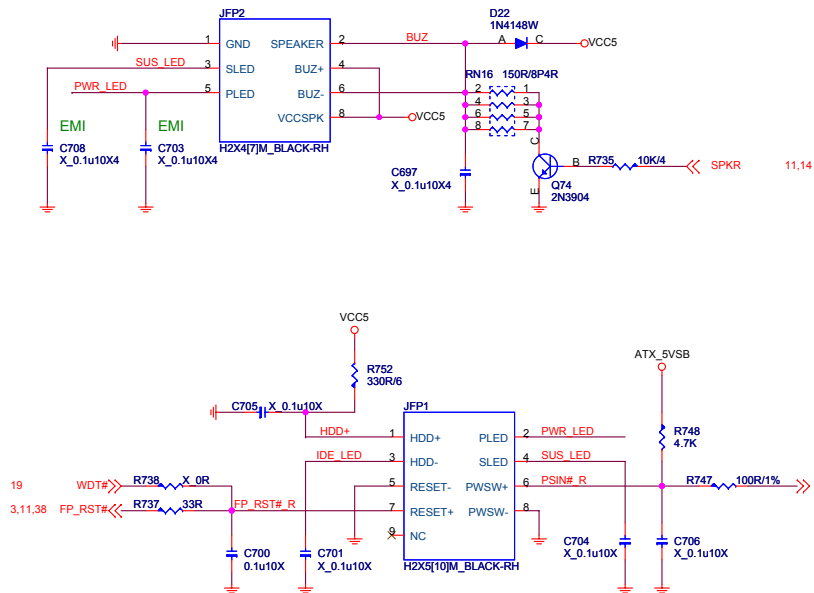
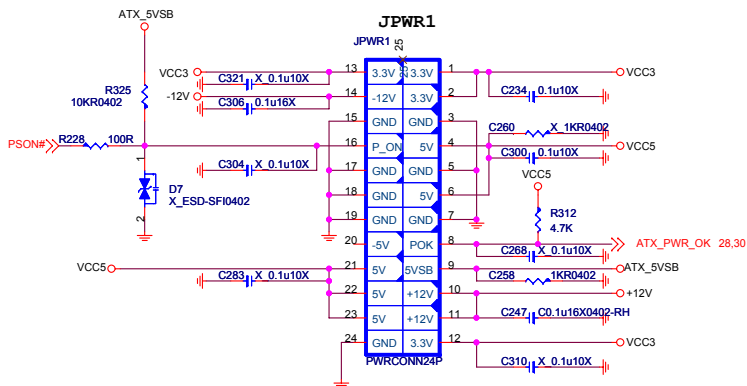


## +3.3V\_ME

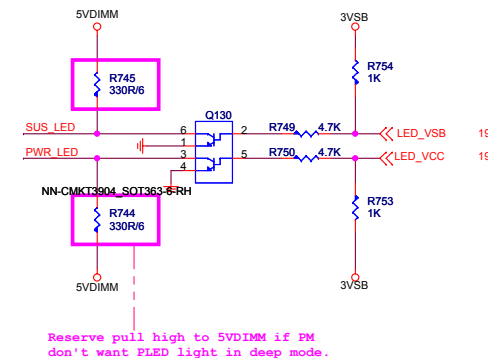


Title			
<Title>			
Size	Document Number		Rev
Custom	<Doc>		<Rev Code>
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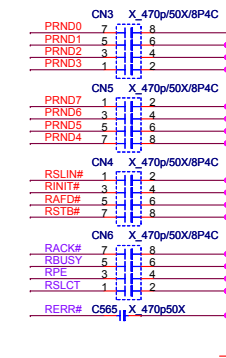
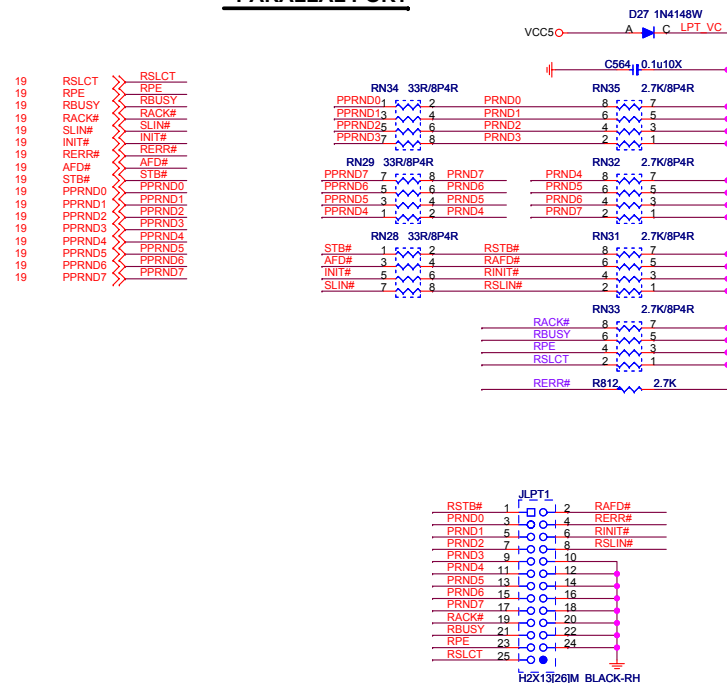
## ATX POWER CONNECTOR



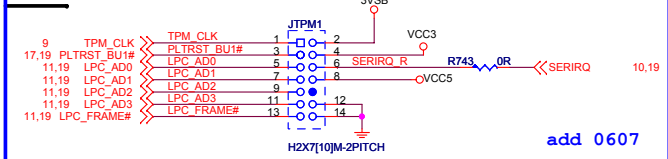
## LED ( for Fintek 71869)

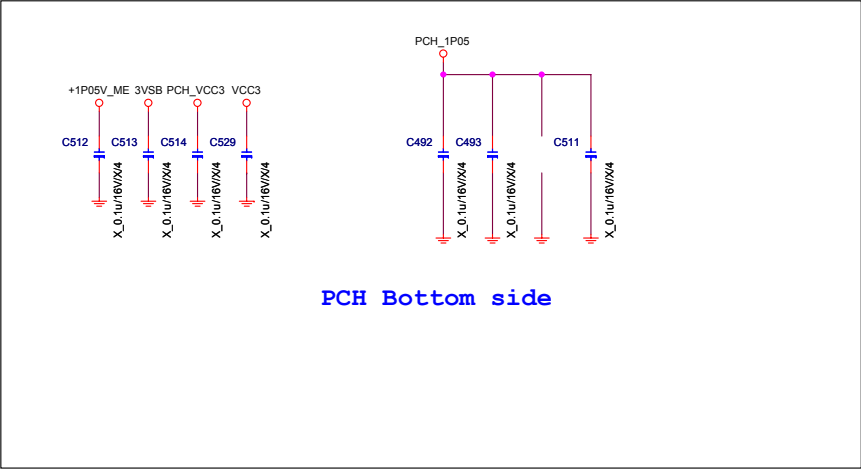


## PARALLAL PORT



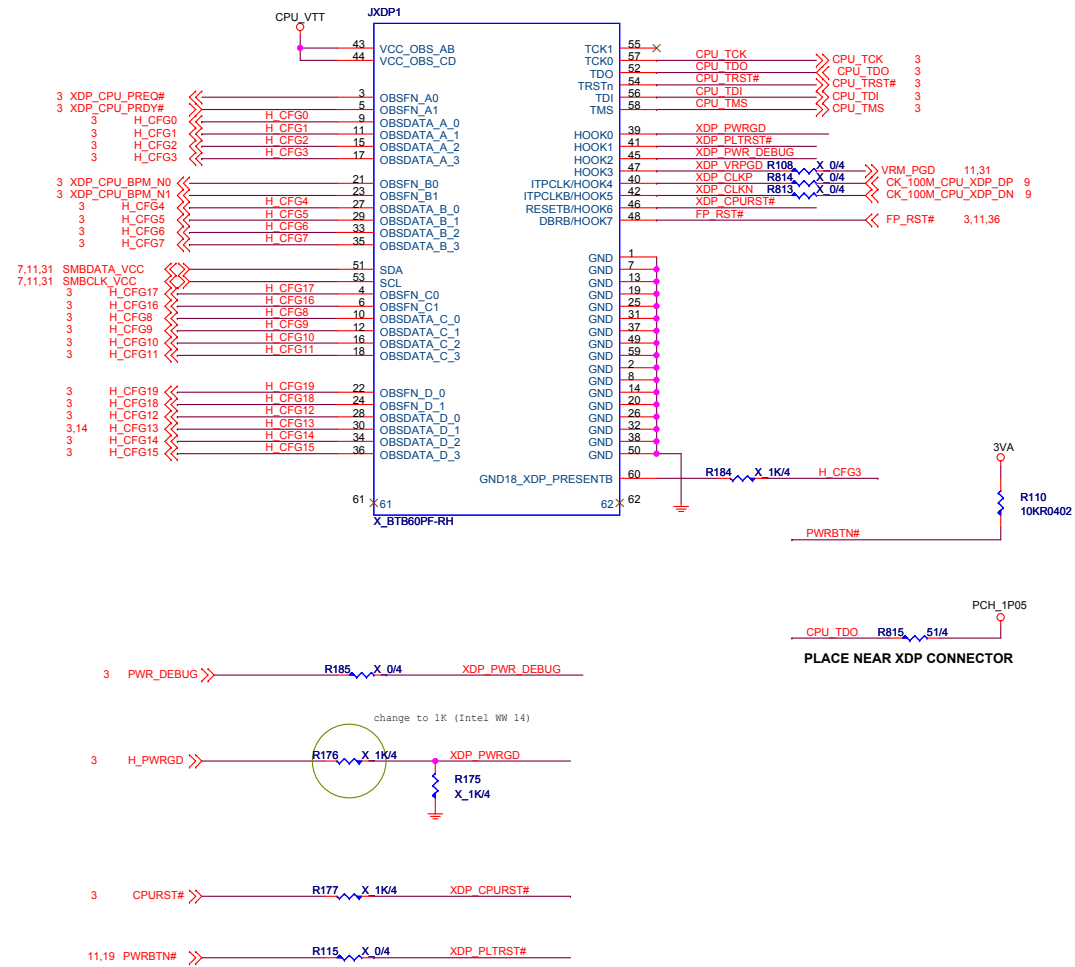
## TPM





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## Reserve debug port 5020

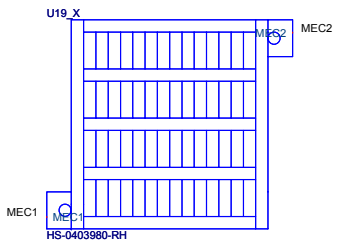


MICRO-STAR INT'L CO.,LTD

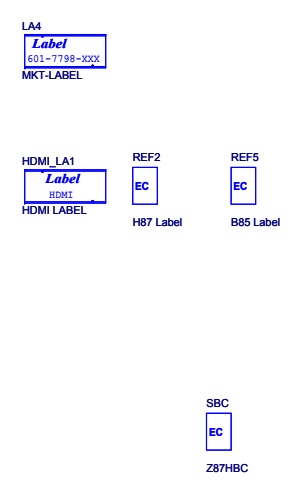
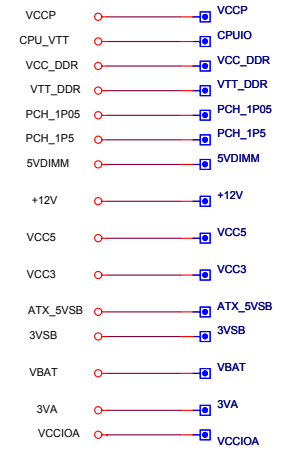
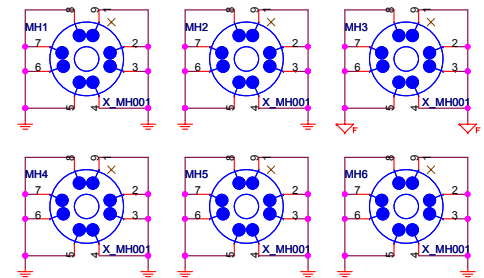
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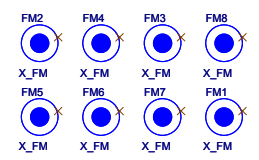
Voltage test point



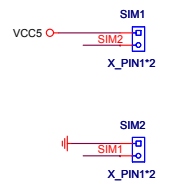
Mounting Holes



Optical Fiducial Marks-120



Simulation



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